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THERMAL STRESS INDUCED VOIDS IN NANOSCALE CU INTERCONNECTS BY *IN-SITU* TEM HEATING

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by

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THERMAL STRESS INDUCED VOIDS IN NANOSCALE CU INTERCONNECTS BY *IN-SITU* TEM HEATING

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Stress induced void formation in Cu interconnects, due to thermal stresses generated during the processing of semiconductors, is an increasing reliability issue in the semiconductor industry as Cu interconnects are being downscaled to follow the demand for faster chip speed. In this work, 1.8 micron and 180 nm wide Cu interconnects, fabricated by Freescale Semiconductors, were subjected to thermal cycles, *in-situ* in the TEM, to investigate the stress relaxation mechanisms as a function of interconnect linewidth. The experiments show that the 1.8 micron Cu interconnect lines relax the thermal stresses through dislocation nucleation and motion while the Cu interconnect 180 nm lines exhibit void formation. Void formation in 180 nm lines occurs predominantly at triple junctions where the Ta diffusion barrier meets a Cu grain boundary. In order to understand void formation in 180 nm lines, the grain orientation and local stresses are determined. In particular, Nanobeam Diffraction (NBD) in the TEM is used to obtain the diffraction pattern of each grain, from which the crystal orientation is evaluated by the ACT (Automated Crystallography for TEM) software. In addition, 2D Finite Element Method (FEM) simulations are performed using the Object Oriented Finite Modeling (OOF2) software to correlate grain orientation with local stresses, and consequently void formation.

According to the experimental and simulation results obtained, void formation in 180nm Cu interconnects does not seem to be solely dependent on local stresses, but a combination of diffusion paths available, stress gradients and possibly the presence of defects. In addition, based on the *in-situ* TEM observations, void growth seems to occur through grain boundary and/or interfacial diffusion. However, *in-situ* STEM observations of fully opened voids post-failure show pileup of material at the Cu grain surfaces. This means that surface or interface diffusion is also very active during void growth in the presence of thermal stresses.

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CHAPTER 1: INTRODUCTION

1.1 MOTIVATION

Since the first integrated circuits were introduced in the 1960s, the microelectronic industry has made tremendous strides in developing faster microelectronic devices by increasing the transistor density through downscaling. This trend has followed Moore's 1965 predictions [1] that the number of transistors on an integrated circuit would double every 2 years (Fig. 1.1). The major drive behind this push has been the increase in consumer demand for computers and computer-related devices, such as multifunctional cellular phones and other handheld devices, high graphic play stations, and computer-enabled home appliances.

Despite the success in producing faster microelectronic devices, the process of downscaling has imposed many challenges over the years. Each time, the industry was been able to meet those challenges through innovative approaches, such as the development of new materials with improved physical properties, new processing techniques, or novel circuit designs. For many years, one of the persistent obstacles to increasing semiconductor speed was the increase in RC delay associated with the aluminum (Al) interconnect-silica (SiO_2) dielectric system. As the interconnect linewidth decreased in parallel with a reduction in transistor size, the increasing RC delay (nearly half the signal delay), which resulted from the electrical resistivity of Al and the relatively high dielectric constant of SiO_2 continued to be an obstacle to

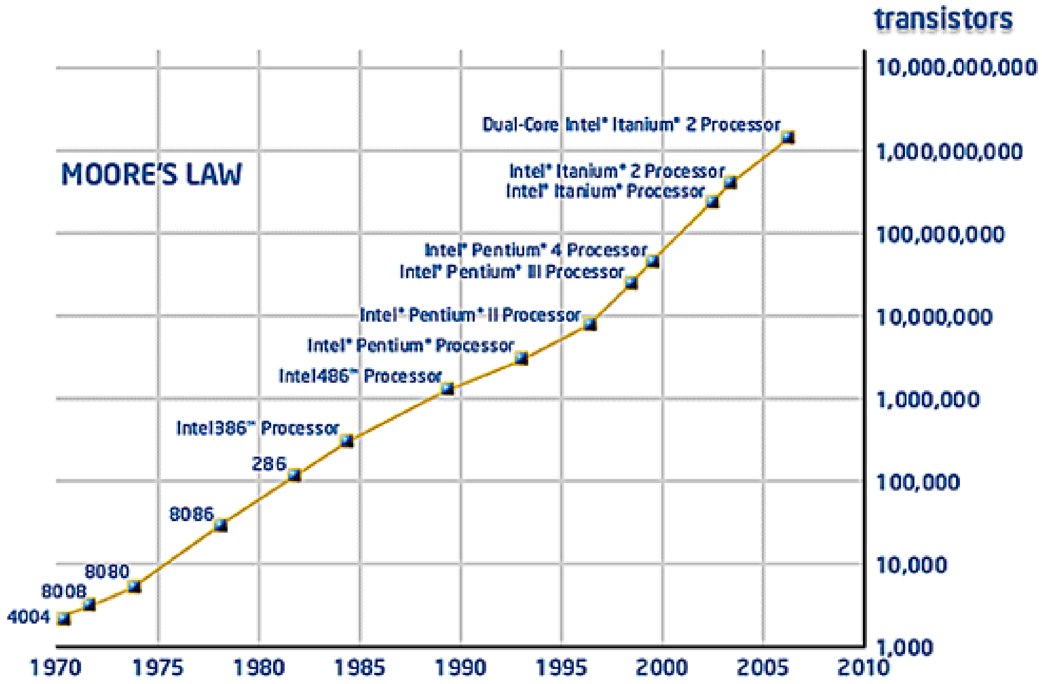

Fig. 1. 1: Moore's Law predicting the number of transistors on an integrated circuit to double every two years [2].

developing faster chips. To address this problem, the industry recognized in the 1980s that Al interconnects had to be replaced with a new metal with lower electrical resistivity. Copper (Cu) was the solution [3].

Cu had long been an obvious choice to replace Al, for not only its superior electrical resistivity, but also its smaller coefficient of thermal expansion (CTE) and better thermal stability (Table 1.1). Though silver (Ag) and gold (Au) were also considered for their better electrical properties, these materials were not cost effective. Superconductors were also an option for use as interconnects, but refrigeration was a deterrent. The first industrial application of Cu as interconnects was finally reported in 1997 [4]. Due to the concerted efforts carried out by researchers in industry and academia to continue downscaling, the current Cu technology, as of 2007, produces a DRAM ½ pitch of 65 nm according to the ITRS Roadmap [5]. Although novel materials, such as carbon nanotubes have been suggested as possible future interconnects, Cu will continue to be used for the time being in conjunction with low-k materials (Fig. 1.2).

When Cu was first proposed to replace Al, it was hoped that the favorable physical properties of Cu, such as a higher melting temperature and a smaller difference in the coefficient of thermal expansion (CTE) between Cu and silicon (Si) would prevent reliability issues that had plagued Al. However, those reliability issues still exist today, in particular, electromigration (EM) and stress-induced-voiding (SIV)

Table 1. 1: Comparison of physical properties between Al and Cu.

	Al	**Cu**
Electrical resistivity [μΩcm]	2.7	2.0~2.2
Thermal conductivity [W/cm/K]	2.37	4.01
CTE (/^{o}C)	23.6×10^{-6}	16.6×10^{-6}
Melting Temperature (K)	933.32	1357.62
Node	>200 nm	<100 nm

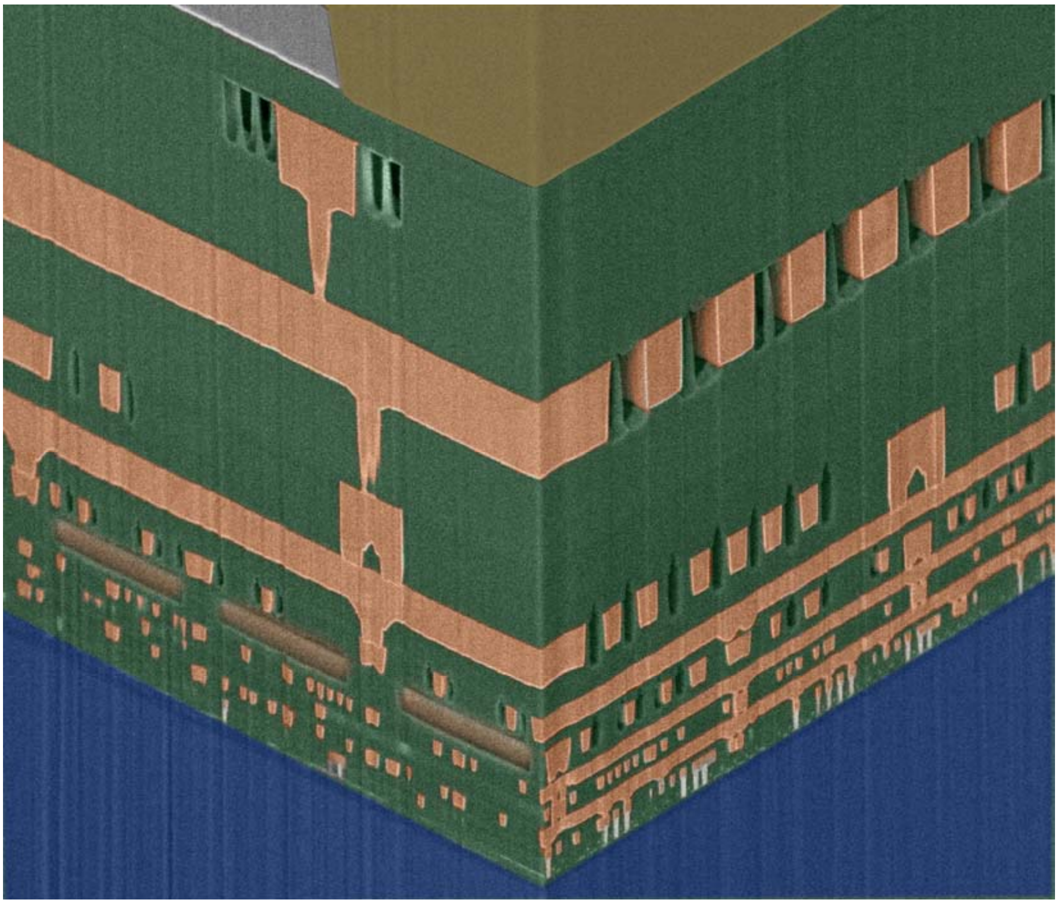

Fig. 1.2: IBM Airgap Microprocessor-empty space used to lower ILD dielectric constant [6].

formation. Understanding EM and SIV is essential in designing future chips, as they can cause unexpected problems during chip usage. EM-induced failure occurs when high current densities in interconnect lines lead to ionic mass transport through the metallic carriers, leading to void formation, hillocks, and mass pileups [7]. SIV occurs when voids nucleate and grow in interconnect lines either during thermal processing, or thermal aging [8].

While numerous studies have been conducted to understand both EM [9-18] and SIV failure [19-28], SIV is still much less understood. In part, this is because the reduction in linewidth changes the state of stresses and grain structure of interconnects, while making it increasingly difficult to conduct analysis at the microstructural level. In addition, the properties of Cu are quite distinct from those of Al, as for example the stacking fault energy and the elastic constants, and thus prior research in Al does not necessarily apply to Cu. In this context, a crucial question arises: *As Cu interconnects are reduced from the micro to nanometer range, and the structural features of Cu approach the nanoscale, how do the overall stress relaxation mechanisms change, and more specifically, how does SIV occur in the presence of thermal stresses?* This dissertation addresses these issues.

1.2 THE APPROACH

To address the effects of thermal cycling on Cu interconnects, *in-situ* Transmission Electron Microscopy heating experiments, ranging from room temperature to approximately 500°C, are conducted in samples of 1.8 micron and 180 nm linewidths. This method allows the observation in real time of dislocation dynamics and/or void formation as a function of Cu interconnect linewidth. Subsequently, to understand SIV in 180 nm Cu interconnects, the grain orientation in these narrow lines is determined by TEM, using the software ACT (Automated Crystallography for TEM). Subsequently, a finite element method-based software, called OOF2 (Object Oriented Finite Element Analysis of Microstructures), uses the crystallographic information acquired by ACT to calculate the local stresses in 180 nm Cu interconnect lines. Finally, a correlation between the TEM observations of void formation, grain orientation and local stresses is established.

1.3 OBJECTIVES AND MAIN CONTRIBUTIONS

1.3.1 Objectives

In order to address the influence of thermal stresses on stress relaxation mechanisms and void formation in nanoscale Cu interconnects, the specific objectives of this dissertation are as follows:

1. To identify the stress relaxation mechanisms in 1.8 micron and 180 nm Cu interconnects by *in-situ* TEM
2. To monitor void formation in 180 nm Cu interconnects by *in-situ* TEM
3. To develop a model for void nucleation in 180 nm Cu interconnects.
4. To identify grain orientations in 180 mm narrow Cu interconnects by TEM and calculate the local stresses in 180 nm narrow Cu interconnects using a Finite Element Method-based software.
5. To establish a correlation between grain orientation, local stresses and void formation in Cu interconnects.

1.3.2 Main Contributions

The main contributions of my thesis are:

1. Using *in-situ* TEM heating to observe the stress relaxation behavior in 1.8 micron and 180 nm Cu interconnects. The stress-temperature relationship of Cu thin films and narrow Cu interconnects show a non-linear behavior [29] and

linear behavior [30], respectively. So far, a correlation between this difference in behavior and the stress relaxation mechanisms in Cu interconnects is not clear. However, by using *in-situ* TEM heating techniques, I am able to observe, in real time, the distinct stress relaxation mechanisms operating in Cu interconnects, under thermal stress. In addition, I am able to identify the roles of the various interfaces (e.g. Cu grain boundary or Cu/diffusion barrier) in the stress relaxation process.

2. Determining the microstructure and crystal orientation of Cu grains in narrow 180 nm Cu lines. This information is critical in understanding void formation behavior, particularly as local stresses, which are a function of crystal orientation are believed to directly affect the void formation behavior. So far, the presence of submicron/nano Cu grain sizes associated with narrow lines has made crystal orientation analysis increasingly difficult. However, this work shows that by using an automated crystallography software (ACT) in conjunction with the Nano-Beam Diffraction (NBD) TEM technique, the crystal orientation of nanoscale Cu grains, as fine as 20 nm, can be indexed.

3. Using a Finite Element Method (FEM) software to simulate local stresses in 180 nm Cu interconnects as a function of grain orientation. This approach and the use of *in-situ* TEM heating techniques allows for a direct correlation between

grain orientation, local stresses and void formation.

4. Modeling void nucleation in 180 nm Cu interconnects based on TEM observations and simulated stresses that are obtained from the aforementioned experiments.

1.4 ORGANIZATION OF THE DISSERTATION

Chapter 2 starts by discussing the current state of understanding of stress relaxation mechanisms under thermal stress in Cu thin films and Cu interconnects. Next a description of void formation and stress-assisted diffusion in Cu interconnects is presented. The thesis then turns to a discussion of grain orientation in Cu interconnects.

In chapter 3, the experimental procedures required to accomplish the objectives of this thesis are discussed. In particular, transmission electron microscopy techniques, such as TEM, STEM, and grain orientation analysis, as well as X-ray diffraction and finite element method-based stress simulations are discussed.

Chapter 4 covers the experimental results, starting with the microstructure analysis of as-received 1.8 micron and 180 nm Cu interconnects. Next, the results obtained from the *in-situ* TEM thermal cycling experiments and the grain orientation analysis in 180 nm lines performed by ACT are presented. The calculation of local stresses using the finite element method software OOF2, based on previous local orientation data, is then laid out. Finally, the results from *in-situ* Scanning Transmission Electron Microscopy (STEM) experiments are presented.

Chapter 5 will provide a discussion on the effects of the dimensions of the Cu interconnects (i.e. the linewidths) on the different stress relaxation mechanisms, as well as discuss the SIV mechanisms based on both experimental and simulation results for 180 nm Cu interconnects presented in Chapter 4. These results will be the basis for modeling void formation to clarify how voids form under thermal stresses in Cu interconnects. The feasibility of the model will be analyzed based on calculations of vacancy concentration under stressed conditions and stress assisted diffusion coefficients. The discussion then turns to void growth behavior, looking at the role of grain boundaries, while performing flux calculations to identify possible diffusion paths. Lastly, *in-situ* STEM results will be discussed to verify if the diffusion paths can be experimentally observed.

This dissertation will conclude with a summary and a discussion of possible future work, which could lead to a better understanding of the SIV behavior. In addition, a novel way of preparing TEM samples for *in-situ* applied electrical current TEM experiments is presented. This technique can be used in conjunction with experimental methodology to better understand EM behavior in Cu interconnects.

CHAPTER 2: STATE OF UNDERSTANDING

2.1 ORIGIN OF THERMAL STRESSES IN CU INTERCONNECTS

Thin metal films/lines, deposited onto a thick Si substrate, are typically subjected to high thermal stresses during processing and/or in service, due to a difference in the coefficient of thermal expansion (CTE) between the deposited metal and the substrate. These thermal stresses can be expressed as:

$$\sigma_0 = \frac{E_f}{1-\nu_f}(\alpha_s - \alpha_f)\Delta T , \qquad (2.1)$$

where α_s and α_f are the coefficients of thermal expansion of the substrate and the film, respectively, E_f is the Young's modulus of the film, ν_f the Poisson's ratio, and ΔT is the temperature change. These thermal stresses in metal layers have been well documented for both Al and Cu films/lines [22,29, 31-43]. When Cu was first investigated for applications as interconnects, the smaller CTE of Cu compared to Al (Table 1.1) was thought to be an advantage for reducing the thermal stresses. However, the higher stiffness of Cu offset this advantage. The product of the biaxial modulus and the difference in the CTE between the metals Cu/Al and Si gives, $M_{Al}\Delta\alpha_{Si-Al} = -2.3MPa^oC^{-1}$ for Al, and $M_{Cu}\Delta\alpha_{Si-Cu} = -2.6MPa^oC^{-1}$ for Cu [33].

Therefore in the case of Cu, the thermal stresses are slightly higher than for Al when subjected to identical thermal treatments.

2.2 SIZE EFFECTS IN STRESS STATE OF CU INTERCONNECTS

Thin metal films deposited on a thick substrate, with or without a passivation layer, exhibit high tensile stresses at room temperature. Upon thermal cycling, the tensile stresses decrease with increasing temperature, eventually transitioning to compressive stresses at high temperatures (Fig. 2.1). Among the two aforementioned types of films, the passivated film has a higher residual tensile stress at room temperature than that of the unpassivated film. In addition, the stress-temperature behavior can vary according to the thickness and grain size of the metal film [44].

Thin metal films are subjected to an isotropic biaxial state of stresses according to equation 2.1, where $\sigma_x = \sigma_y = E\Delta\alpha\Delta T(1-\upsilon)$, and $\sigma_z = 0$. However, in the case of unpassivated metal lines, an anisotropic biaxial state of stresses is typically observed where $\sigma_x \neq \sigma_y$, and $\sigma_z = 0$, while in passivated lines a triaxial stress state where $\sigma_x \neq \sigma_y \neq \sigma_z$, and $\sigma_z \neq 0$ is normally present (Fig. 2.2) [8,45]. Fig. 2.3 shows the changes in the stress state from biaxial stress to triaxial stress as the line's thickness-to-width ratio varies from small (wide lines) to large (narrow lines) values. It can be seen that as the thickness-to-width ratio increases, σ_z becomes more significant, and the stresses become quasi-hydrostatic.

In addition to changes in stress states (from an isotropic biaxial stress for thin films to a triaxial stress state for passivated narrow lines), a variation in dimensions of

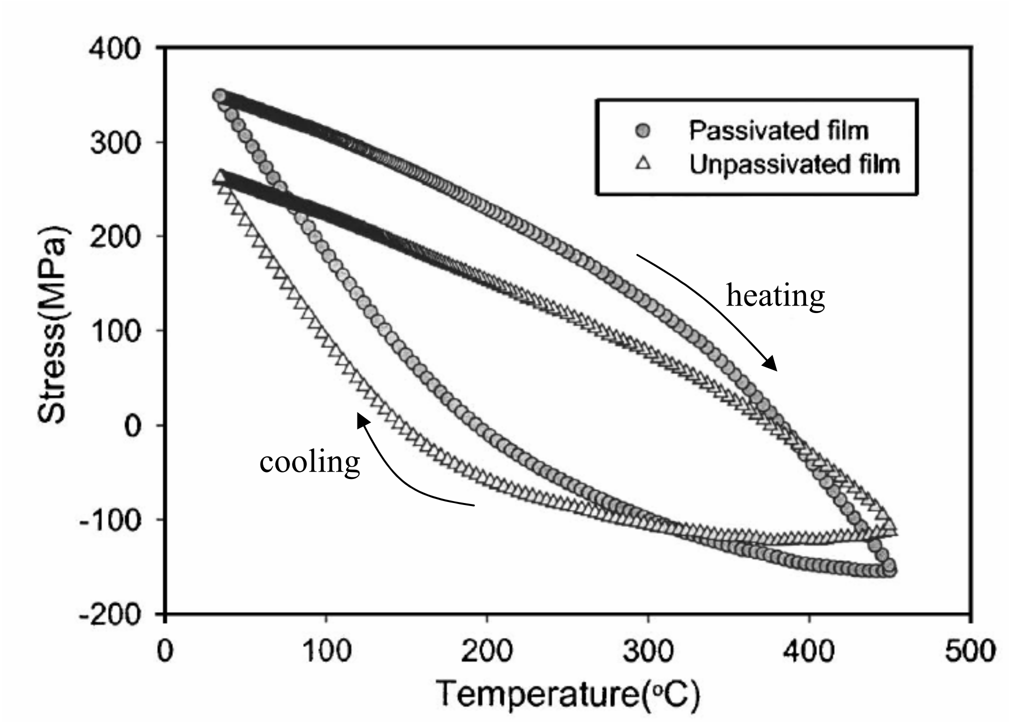

Fig. 2.1: Thermal stresses in 1 micron electroplated passivated and unpassivated Cu films [46].

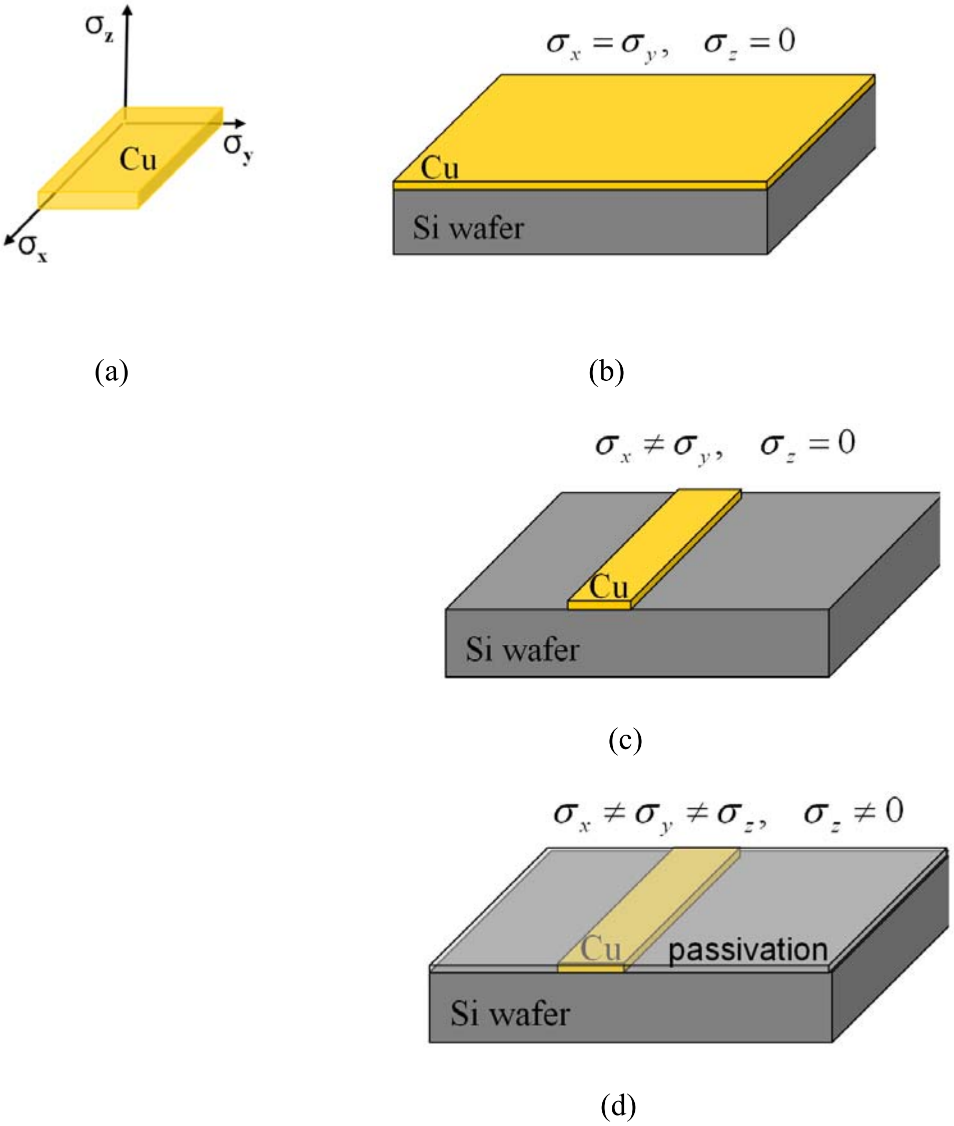

Fig. 2.2: Change in stress states for different metallization configurations [8]. (a) reference system used in this work (b) Isotropic biaxial stress state in films (c) anisotropic biaxial stress state in unpassivated lines (d) triaxial stress sate in passivated lines

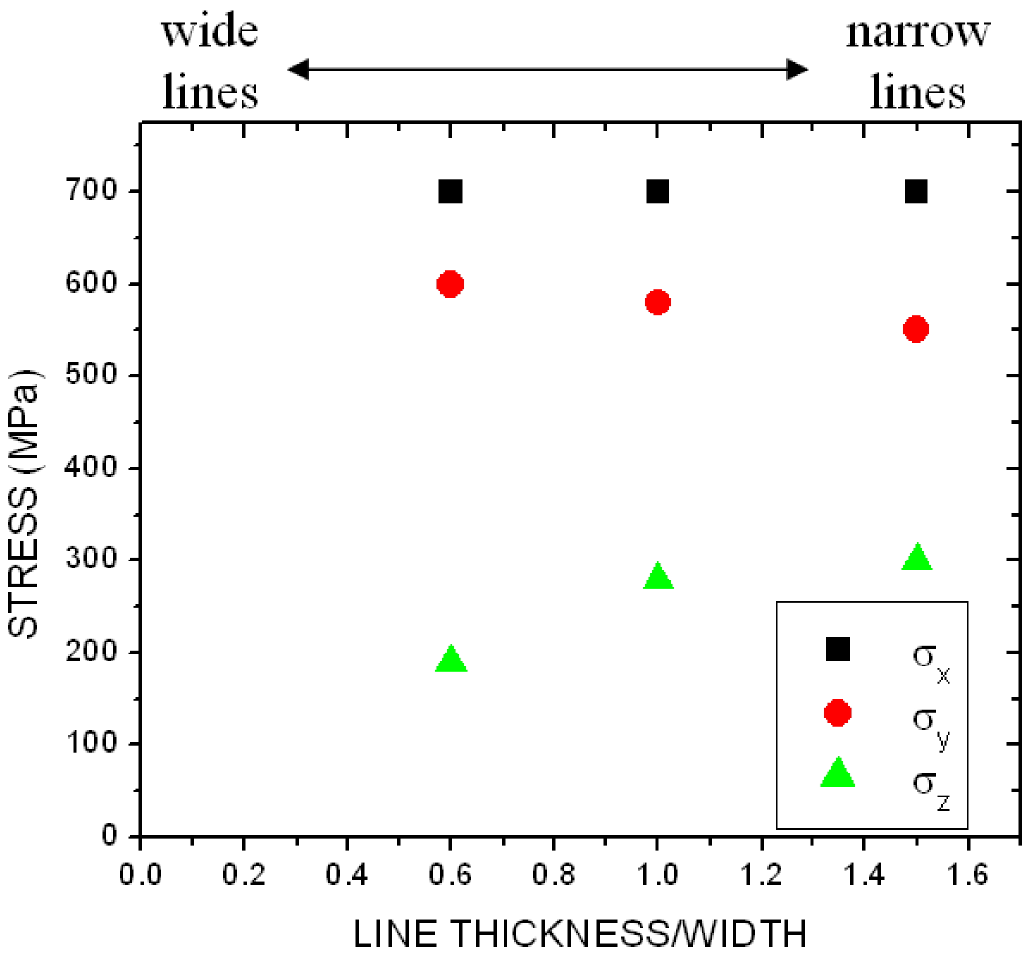

Fig. 2.3: Normal stresses in passivated Cu interconnects as a function of thickness-to-width ratio [47].

the metal layers also show distinct differences in the stress-temperature behavior during thermal cyclic tests. This is shown in Fig. 2.1 where the stress-temperature behavior for film shows a non-linear trend, while narrow passivated interconnects show a linear change in stress as a function of temperature in Fig. 2.4. This indicates that while thin films undergo plastic yielding, the deformation behavior in passivated narrow lines is largely elastic. The lack of plastic yielding under such quasi-hydrostatic stresses can have an impact on the stress relaxation mechanisms, due to the fact that dislocation motion is unlikely to occur. In such cases (passivated narrow lines), stress relaxation can be achieved by void formation. [45]. This can be qualitatively understood by looking at the von Mises Criterion. For plastic deformation to occur, the von Mises Criterion (σ_v) given by

$$\sigma_v = \frac{1}{\sqrt{2}}\left[(\sigma_x - \sigma_y)^2 + (\sigma_y - \sigma_z)^2 + (\sigma_z - \sigma_y)^2\right]^{\frac{1}{2}} \qquad (2.2)$$

must exceed the yield strength σ_Y. For thin films, $\sigma_v = \sigma_x (= \sigma_y)$. Thus if $\sigma_x > \sigma_Y$, yielding will occur. For passivated narrow lines, assuming a perfect hydrostatic case where $\sigma_x = \sigma_y = \sigma_z$, and $\sigma_v = 0$, yielding will not occur. In the case of a quasi-hydrostatic stress state (i.e. a triaxial stress state where $\sigma_x \neq \sigma_y \neq \sigma_z$, and $\sigma_z \neq 0$), the von Mises Criterion will be low, and yielding will be difficult.

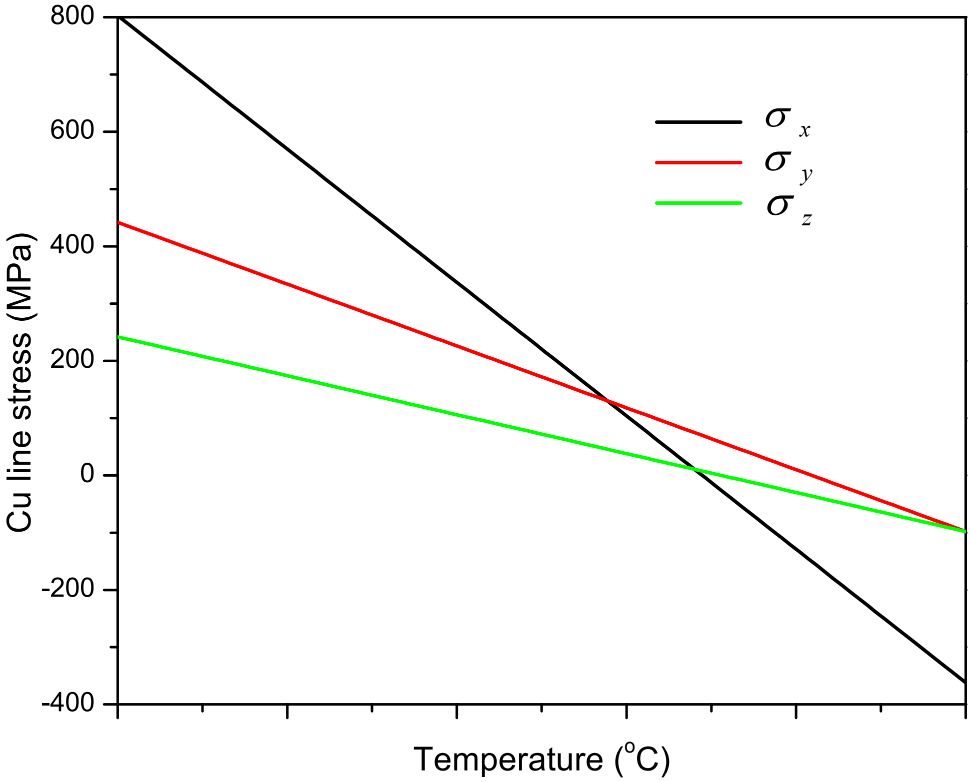

Fig. 2.4: Stress-temperature relationship for 0.2 micron Cu lines in SiOF dielectric layer based on XRD data. Recreated from graph in [37].

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2.3 STRESS RELAXATION MECHANISMS OF CU INTERCONNECTS UNDER THERMAL STRESS

2.3.1 Dislocation mechanisms in thin Cu films

When thin films are subjected to thermal stresses, the strains are typically relieved through dislocation mechanisms [36,48-53]. These mechanisms, investigated on various films, show a behavior different from that of bulk materials. In thin films, the grain structure is generally columnar, and the dislocations observed are threaded dislocations, extending from the film/substrate interface to the film/passivation interface (Fig. 2.5). These dislocations, in the presence of a passivation layer, become easily pinned at the interfaces, and have difficulty gliding under the influence of stress. This behavior has been observed for the case of the Al /Al_2O_3 interface [36]. As a result, passivated thin films generally have higher yield stresses than unpassivated or thicker films. But depending on the type of the passivation material, the metal thin film/passivation layer interface can behave quite differently, as for example the case of Cu and amorphous SiN_x interface, where the interface was reported to be a sink source for dislocations [31]. Thus, the role of the interface will be dependent on the nature of the dislocation-interface interaction and the structure/properties of the interface.

In ultrathin, 200 nm, unpassivated, Cu films, unexpected dislocation motion was observed by *in-situ* TEM heating experiments [49]. In particular, dislocations

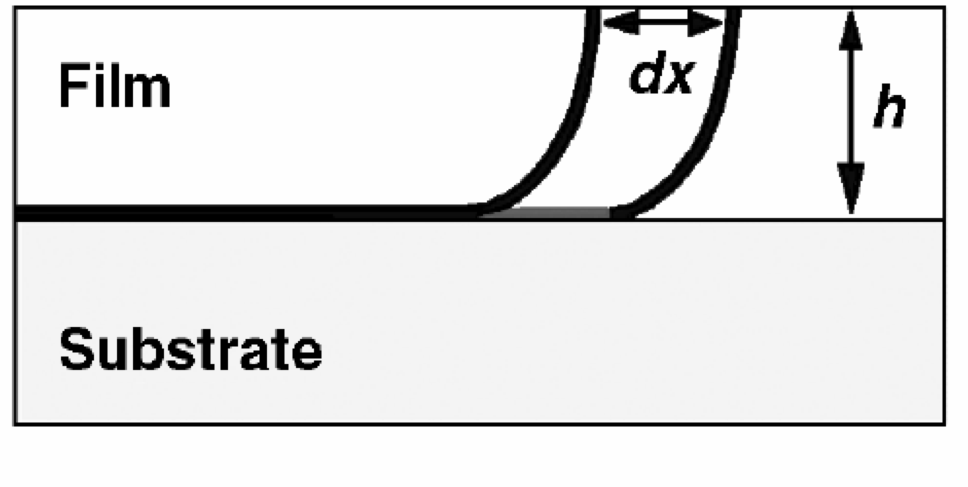


Fig. 2.5: Threaded dislocations in thin films [36]. 'h' is the film thickness, and 'dx' is the dislocation segment length needed to be created when the dislocation moves by the distance dx.

were seen to nucleate at Cu triple junctions in a grain roughly 700 nm in diameter, further gliding into the crystal along a (111) type plane, pushed by newly nucleated dislocations. These results showed that plastic deformation in thin films changed from threading dislocations in Cu films over 400 nm to parallel gliding dislocations in films under 400 nm. These reports indicate that the stress relaxation through dislocation dynamics is a complex process, determined by the type of interfaces available and the film thickness.

2.3.2 Void nucleation and growth under thermal stress

In addition to stress relaxation through dislocation nucleation and motion, Cu interconnects can exhibit stress-induced void formation. The latter mechanism has been first reported in 2.5 to 3.5 micron wide Al lines, by Curry *et .al.* [54] and Yue *et. al.* [55]in the mid 1980s (Fig. 2.6). Since then, stress-induced void formation has been studied intensively in Al [21,26,27,56-62] and Cu [20,24,25,63-67] for films [20, 24] and lines [25,63-67].

In addition, several papers have studied the diffusivity along various interfaces (Cu grain boundary, Cu/passivation interface, and Cu/DB interface) and its' role in stress relaxation behavior in Cu films [46,68,69]. SIV occurs during processing or/and in use, when the interconnect samples are subjected to one or more thermal cycles. Once these voids form, the current density can greatly increase due to a reduction in cross sectional area. This is turn can lead to void growth and failure

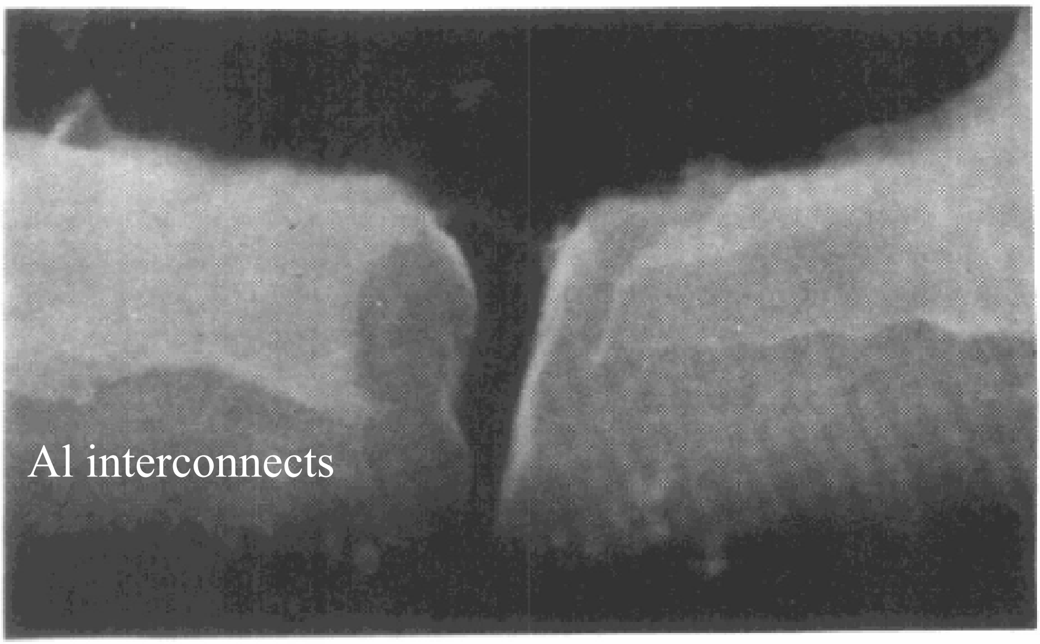


Fig. 2.6: Stress-Induced-Void formation (SIV) in Al lines [54].

through EM, in addition to SIV [8].

A qualitative understanding of the SIV behavior in interconnects can be inferred by looking at changes in stress and diffusion rate with increasing temperature. In general, the stress of metal films on a stiff substrate decreases with increasing temperature. On the other hand, at higher temperatures, the atomic mobility and consequently the diffusivity rate increase. Therefore, the temperature at which void formation occurs is a compromise between sufficiently high stresses and significant diffusion (Fig. 2.7).

In general, stress-induced void formation occurs in two steps, namely nucleation and growth. Although void nucleation is not fully understood, the typical approach is to perform a thermodynamic (energetic) analysis of void nucleation. In this fashion, the change in Gibbs free energy for void nucleation can be expressed as

$$\Delta G = \Delta G_e + \Delta G_s + \Delta G_g \tag{2.3}$$

where ΔG_e is the change in elastic energy, ΔG_s the change in surface energy, and ΔG_g the change in grain boundary energy associated with the nucleation of a void. A careful analysis of equation (2.3) reveals that the change in Gibbs free energy is a function of void size. As shown in Fig. 2.8, ΔG increases with void size before reaching a maximum at a critical particle size, followed by a monotonic decrease in

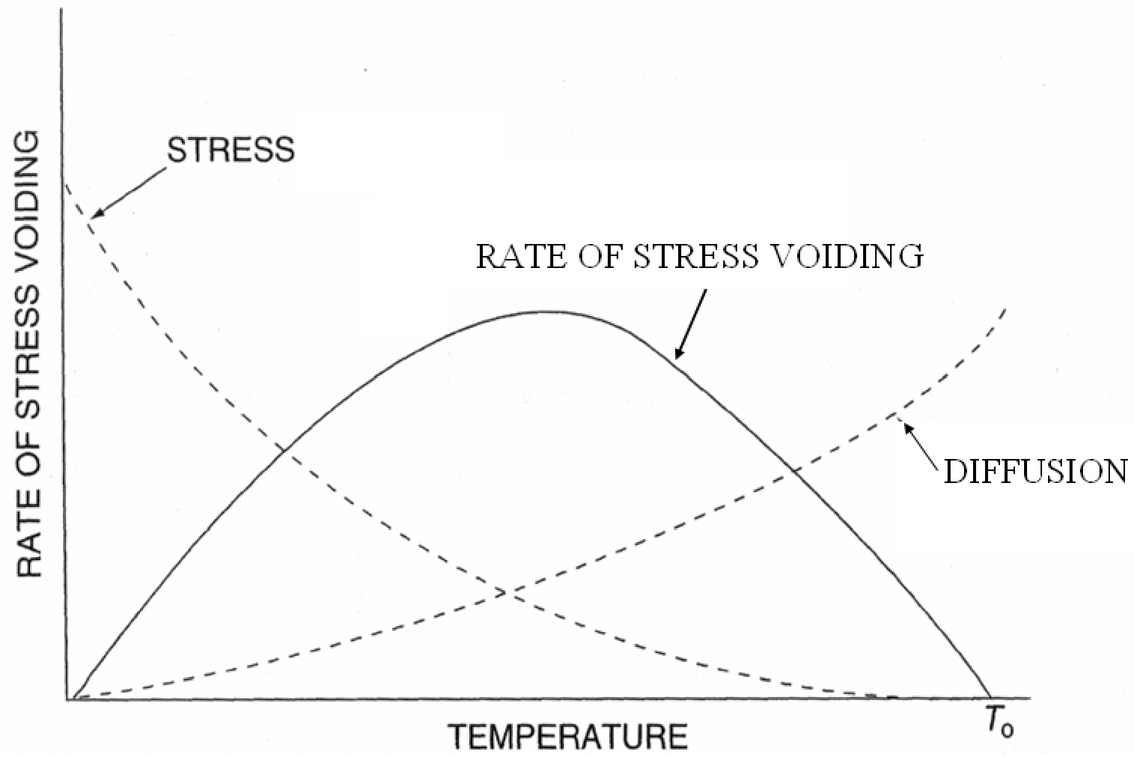


Fig. 2.7: Stress induced voiding as a function of temperature with a decrease in stress and an increase in diffusivity with temperature. The maximum rate of SIV occurs at an intermediate temperature. [8].

Gibbs free energy with a further increase in void size [56]. The presence of a maximum in the Gibbs free energy function means that an energy barrier (ΔG_c) must be overcome before a void with critical size can be stable and grow.

In the case of Al interconnects, Gleixner *et. al.* have studied in detail the energetics of void nucleation considering the effects of site geometries, interfaces, and interface flaws [21]. The models suggested include homogeneous nucleation of voids by purely statistical vacancy condensation, nucleation at a grain boundary, nucleation at the line sidewall, and nucleation at an interface notch. Based on the calculations, Gleixner *et. al.* [21] concluded that the nucleation rates for each of the above nucleation sites were too small to be realistic, and therefore void nucleation by vacancy condensation should not expected in passivated interconnect lines. On the other hand, the paper considered the formation of vacancies in sidewall notches (defects from processing) as the cause of void formation. If R_p is the radius of the circular contaminant patch (Fig. 2.9), the critical stress $\sigma *$ required to overcome the energy barrier can be given by

$$\sigma * = \frac{2\gamma_{Al} \sin \theta_c}{R_p} \qquad \text{for} \quad \theta_c < \pi / 2 \tag{2.4}$$

where γ_{Al} is the free surface energy of Al and θ_c the equilibrium contact angle. Based

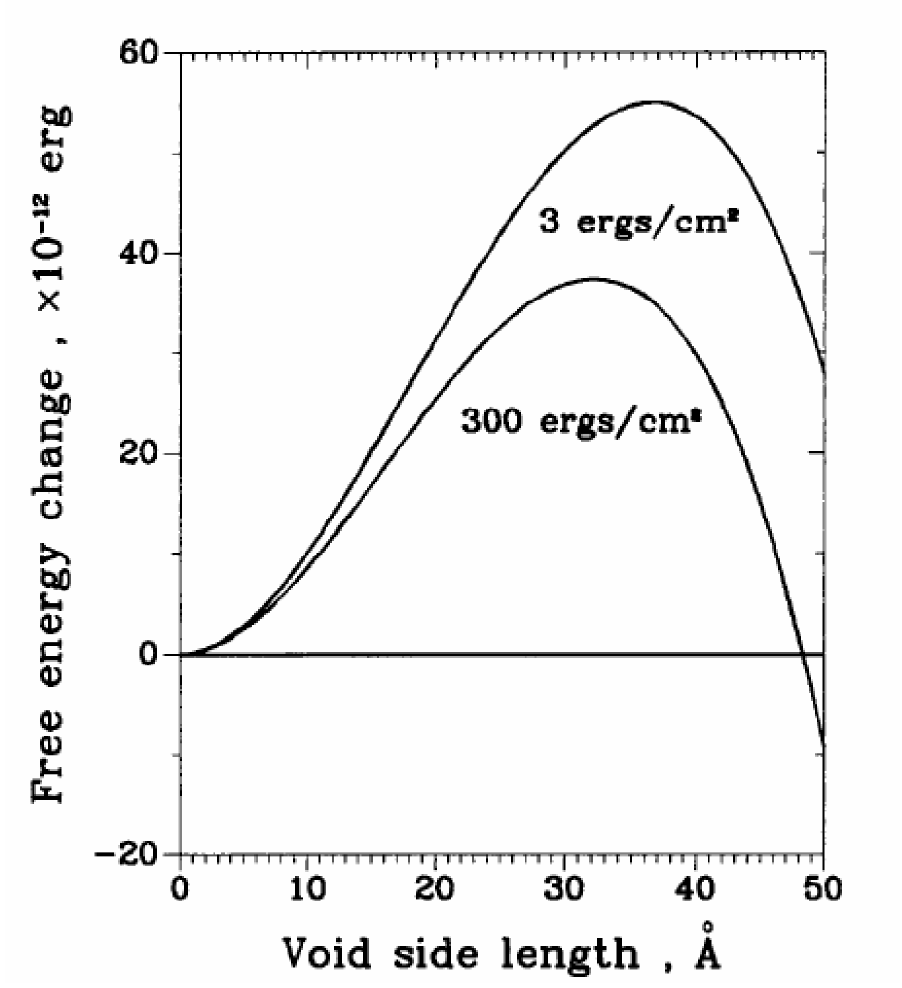
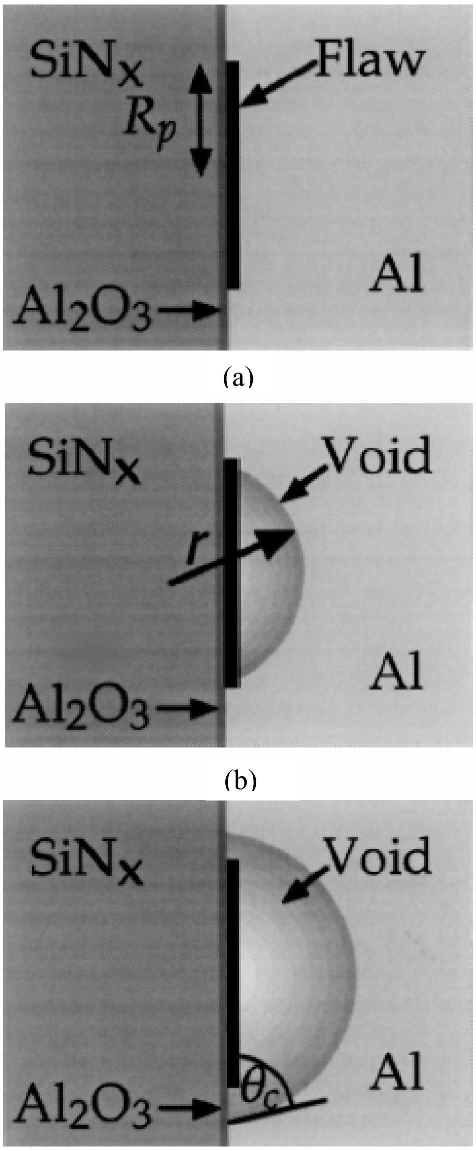


Fig. 2.8: Change in free energy as a function of void size [56].



(a) (b) (c)

Fig. 2.9: The process by which an interface flaw becomes a void. (a) initial flaw at zero stress (b) applied stress driving Al surface to bow to radius of curvature r. The flaw leaves the patch (c) [21].

on the results obtained from equation (2.4), the authors concluded that with a typical thermal stress of 500MPa, void nucleation can occur from a flaw as small as 4nm in the absence of a nucleation barrier. If instead a stress of 2 GPa is assumed, flaws as small as 1 nm are sufficient for void nucleation to occur [21], indicating that void nucleation at a flaw at the Al/Al_2O_3 interface might be a plausible mechanism for void nucleation.

In terms of void growth, there are many possible factors that partake in affecting SIV in interconnects, including defects, stress, and passivation layer. Among these, the presence of thermal stresses is regarded as the dominant factor. For Al, void growth has been assumed to occur through grain boundary diffusion, under creep conditions. The various models are discussed in detail by Okabayashi [27]. In general, the flux (j) of atoms under a chemical potential gradient is given by

$$j = -\frac{D}{\Omega kT}\nabla(\mu - \mu_v) \tag{2.5}$$

where D is the diffusion coefficient, Ω the atomic volume, k Boltzman’s constant, T the temperature, μ and μ_v the chemical potential for atoms and vacancies, respectively. As shown in equation (2.5), the gradient in chemical potential difference between atoms and vacancies is ultimately driving void growth. While the diffusion coefficient (D) in the absence of stress is given by

$$D = D_o \exp\left(-\frac{Q_d}{kT}\right), \tag{2.6}$$

where D_0 is the pre-exponential factor and Q_d the activation energy. In the presence of stress, the diffusion coefficient can be expressed as

$$D_s = D \exp\left(-\frac{\sigma\Omega}{kT}\right) \tag{2.7}$$

where σ is the stress. Furthermore, in the presence of stress, the difference in chemical potential between atoms and vacancies is given by

$$\mu - \mu_v = \mu_o - \Omega\sigma \tag{2.8}$$

where μ_o is the chemical potential for an unstressed state. Assuming the void grows by one-dimensional atomic flux, and inserting equation (2.8) into equation (2.5) gives

$$j = \pm \frac{D_S}{kT} \frac{d\sigma}{dx} \tag{2.9}$$

The vacancy concentration (N_v) is also affected by stress, and thus can be expressed as

$$N_v = N_o \exp\left(\frac{\Omega\sigma}{kT}\right) \cong N_o\left(1 + \frac{\Omega\sigma}{kT}\right) \qquad \text{for } \frac{\Omega\sigma}{kT} < 1 \tag{2.10}$$

where N_0 is the vacancy concentration in an unstressed state. If one dimensional flux occurs and atoms originally in the void migrate into the grain boundary to be accommodated, then

$$\frac{d\delta}{dt} = -\Omega\delta_b \frac{dj}{dx} \tag{2.11}$$

where $d\delta$ is the change in thickness of the grain boundary, t the time, and δ_b the grain boundary thickness (Fig. 2.10). Due to the atomic flux, the stress is relaxed in the regions adjacent to the grain boundary, which can be expressed as a function of time as

$$\sigma(t) = \sigma_0 - M\frac{\delta(t)}{x_b} \tag{2.12}$$

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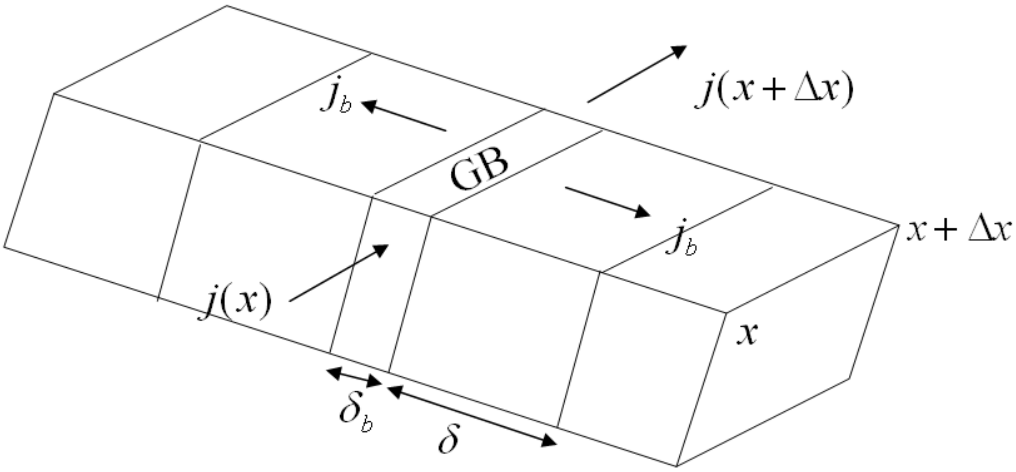

Fig. 2.10: Accommodation of mass at grain boundary (GB). J is the atomic flux, j_b the flux of atoms deposited at the GB, δ_b the grain boundary thickness, δ the grain boundary thickening (adapted from [27].)

where σ_0 is the initial stress (thermal stress), *M* is the lumped elastic constant of the line, and x_b is the distance over which stress relaxation due to grain boundary thickening. By differentiation of equation (2.12) with respect to t, and inserting the result into equation (2.11) gives

$$\frac{d\sigma}{dt} = \frac{M\Omega\delta_b}{x_b}\frac{dj}{dx} \tag{2.13}$$

Since $j = \frac{D}{kT}\frac{d\sigma}{dx}$, then $\frac{dj}{dx} = \frac{D}{kT}\frac{d^2\sigma}{dx^2}$ and by inserting $\frac{dj}{dx}$ into equation (2.13) yields

$$\frac{d\sigma}{dt} = \frac{M\Omega\delta_b D_b}{x_b kT}\frac{d^2\sigma}{dx^2} \tag{2.14}$$

where D_b is the grain boundary diffusion coefficient. In general, equation (2.14) can be written in the form

$$\frac{d\sigma}{dt} = \frac{CM\Omega\delta_b D_b}{x_b kT}\frac{d^2\sigma}{dx^2} \tag{2.15}$$

where C is a diffusion model dependent factor. Assuming that one void exists in an infinitely long line, then $\sigma(x,t)$ can be derived by taking as boundary conditions $\sigma_0 = \sigma(\infty,t) = \sigma(x,0)$, giving

$$\sigma(x,t) = \sigma_0 erf\left[\left(\frac{kTt}{CM\Omega\delta_b D_b}\right)^{\frac{1}{2}}\frac{x}{2}\right] \tag{2.16}$$

Since from equations (2.12) and (2.13),

$$\delta(x,t) = \frac{x_b\sigma_0}{M}\mathrm{erfc}\left[\left(\frac{kTt}{CM\Omega\delta_b D_b}\right)^{\frac{1}{2}}\frac{x}{2}\right] \tag{2.17}$$

The void volume can be given as

$$V(t) = 2L_b WH\int_0^{L/2}\delta(x,t)dx \tag{2.18}$$

or, $$V(t) = 2\Omega S\int_0^t j_{av}(0,t)dt = \frac{2\Omega D}{kT}\int_0^t \frac{d\sigma(x,t)}{dx}\Big|_{x=0} dt \tag{2.19}$$

where L_b is the total length of grain boundary per unit area of film, $\pm L/2$ the distance over which stress relaxation occurs due to growth of a single void, S is the total cross sectional area of diffusion paths in the cross-section of the line, and j_{av} is the flux averaged over diffusion paths in the cross-section of the line.

Assuming the growth of a single void to result in a uniform stress relaxation over the distance $\pm L/2$ away from the void, the maximum void volume V_m is given by

$$V_m = \frac{3(1-2\nu)V_0}{E}\left(\sigma_0 - \sigma_e - \sigma_p\right) \tag{2.20}$$

$$V_0 = WHL \tag{2.21}$$

where ν is the Poisson's ratio, σ_e the yield stress, σ_p the stress relaxed by plastic deformation, and V_0 the volume of the segment of the Al that undergoes stress relaxation. V_m in equation (2.20) gives an approximation of the void volume for the real case where stress relaxation may not be uniform.

Physical models were developed by Yost [58, 70] for void growth in equiaxed columnar grains (Fig. 2.11), where mass transport is accommodated by grain boundaries. According to these models, the tensile stress relaxes along the width of the line, and over time along the length of the line as well. The void size *a*(t) may be obtained from equation (2.20) which gives the maximum void volume. This gives

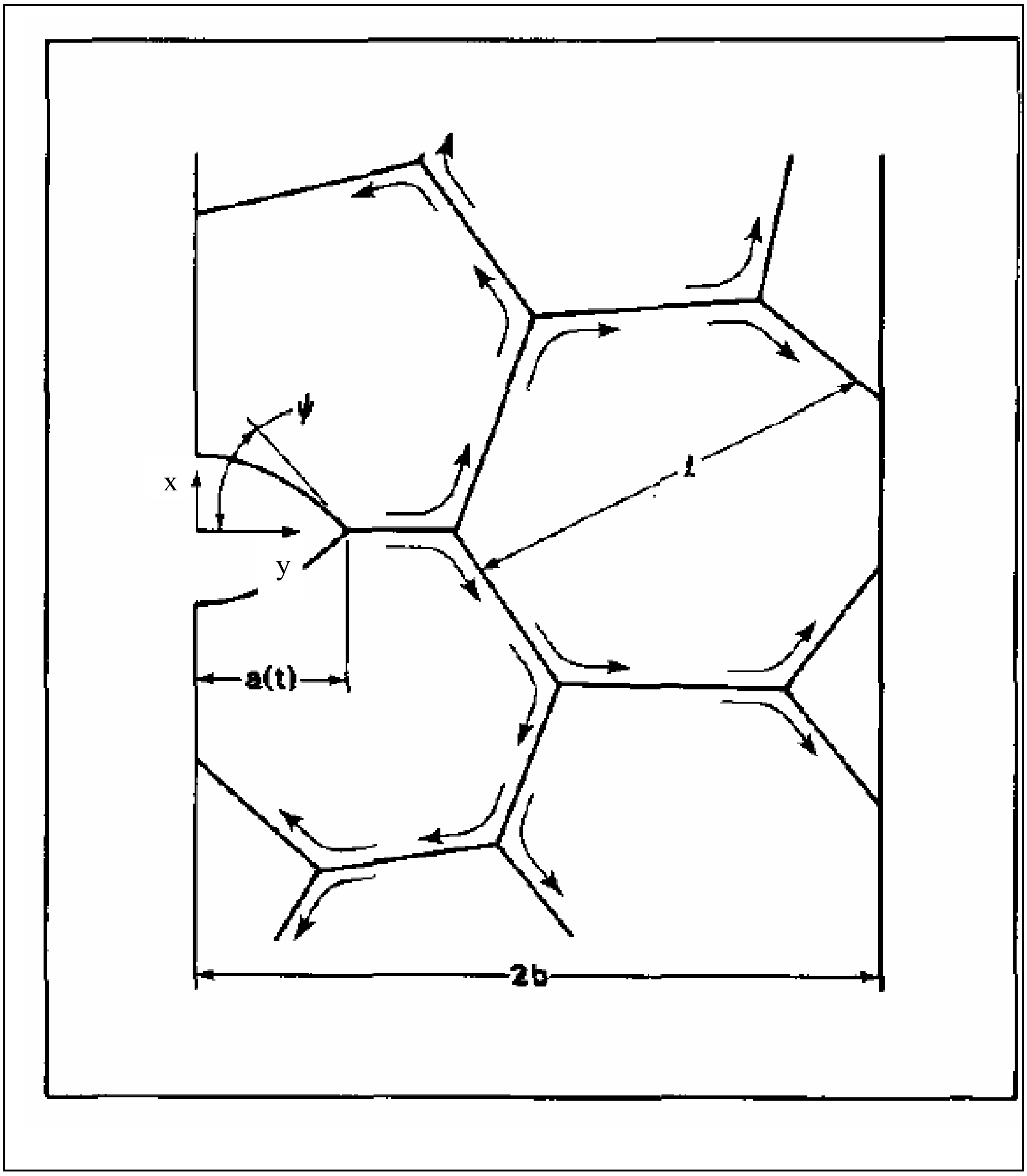

Fig. 2.11: Wedge-shaped void of size *a*(t) growing via grain boundary diffusion in a columnar line [58].

$$a(t) = \left(\frac{2w\sigma 0}{h}\right)^{0.5} \left(\frac{2(1-\nu)\Omega\delta_b D_b t}{gEkT}\right)^{0.25} \tag{2.22}$$

where h is a shape factor (~1).

Since these models are based on multigrained equiaxed columnar grains, and this thesis revealed the presence of near bamboo structures for 180 nm interconnects, we will now look at a physical model developed for a bamboo structure line. For bamboo structure lines, grain boundaries only exist along the width of the line, and thus, the void growth rate can be determined by diffusion of vacancies along this grain boundary. Yost developed a numerical model for voids lying on each edge of a bamboo grain boundary [57]. It was assumed that Al diffuses through the void surface into the connecting grain boundary (Fig. 2.12). This was thought to decrease the stress instantaneously in the longitudinal direction over a direction L/2 on both sides of the grain boundary. Consequently, the longitudinal stress σ_x develops along the linewidth direction (y-direction). If Al diffusion on the surface of the void is faster than diffusion at the grain boundary, the void growth rate will depend on the diffusion rate at the grain boundary. The flux, j, on the grain boundary then becomes;

$$j(y,t) = \frac{D_b}{kT}\frac{d\sigma_x(y,t)}{dy} \tag{2.23}$$

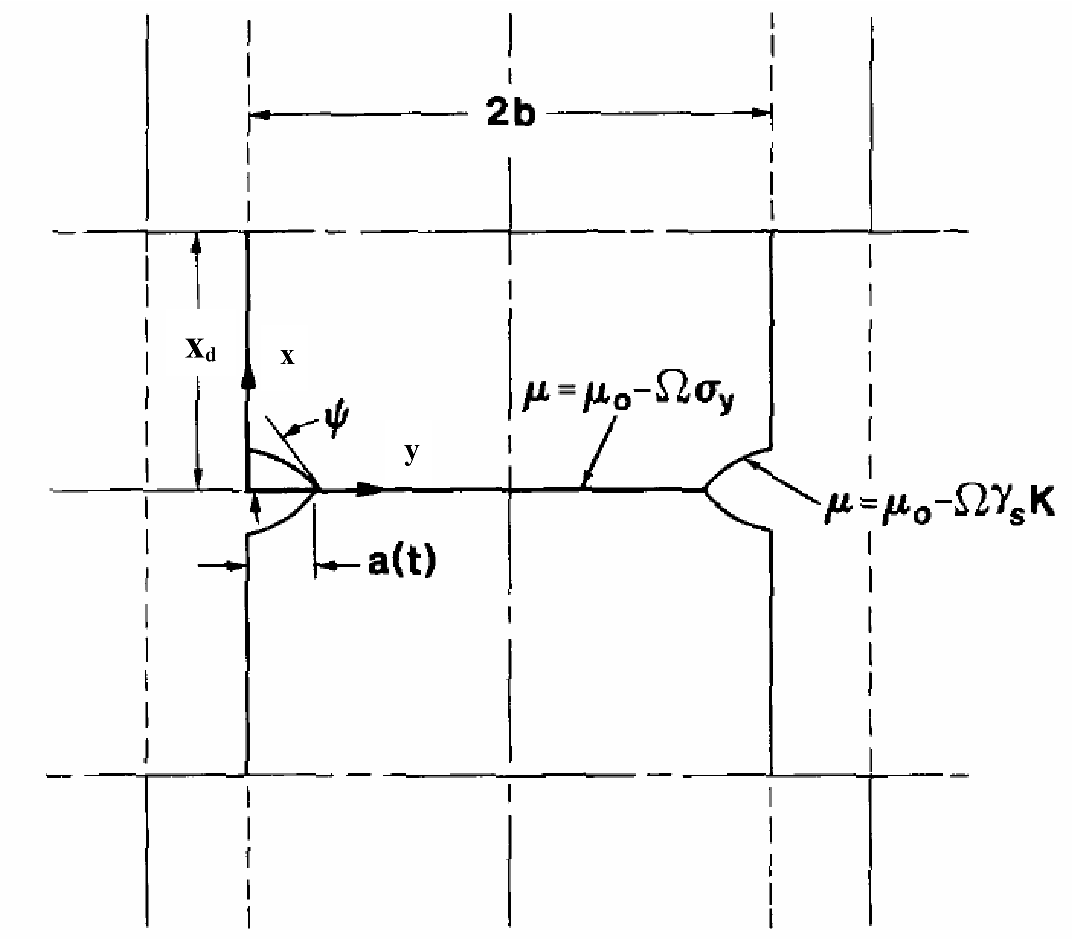

Fig. 2.12: Conductor line and void geometry showing appropriate chemical potential (μ and μ_0 are the chemical potential and chemical potential under zero stress respectively) and relaxation distance y_d. ψ is the void angle, γ_s the surface energy and K the curvature. The other terms have the same meaning as before [70].

In other words, the equation above shows that the driving force for void growth is proportional to the gradient of the longitudinal stress across the width of the line. Following similar arguments given from equations (2.5) to (2.13), gives

$$\frac{d\sigma_x(y,t)}{dt} = \frac{2EB}{(1-\nu)L}\frac{d^2\sigma_x(y,t)}{dy^2} \tag{2.24}$$

The resulting graph for a 3 micron wide line (100 microns long) at t=0 is shown in Figure 2.13. The graph shows a decrease in stress from the edge to the middle of the line. This stress at the edge is expected to be the driving force for void growth.

Hu also developed models for explaining void growth in bamboo-structured Al lines, but in this case grain boundaries were considered to be regularly spaced by a distance *g* [61]. The following two assumptions were considered in Hu's model, i) The diffusion of Al along the grain boundary is fast enough, such that stress relaxation is complete after a negligibly short time, and ii) Void growth continues via mass transport through bulk diffusion, cascading down sequential tiers of grain boundaries, resulting in a layer of extra mass at each grain boundary for stress relaxation.

Based on this second assumption, the flux j_n across the n*th* grain, for the (n-1)*th* to the n*th* grain boundary is given by

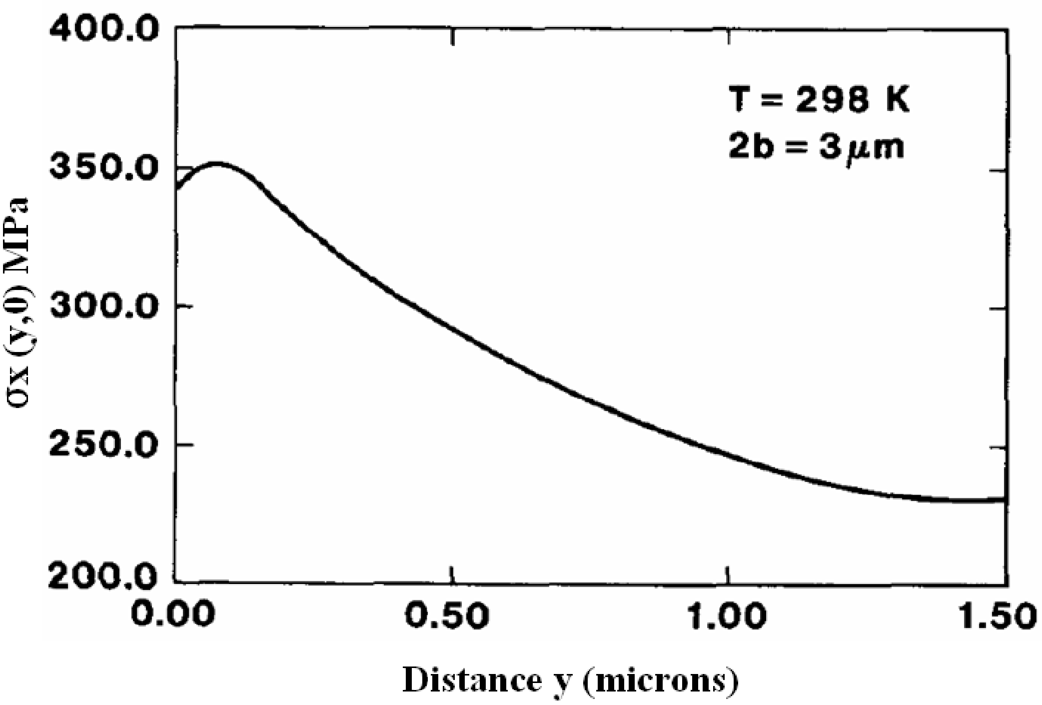

Fig. 2.13: Change in stress along the y axis of the interconnect from the edge (y=0) to the middle of the line (y=1.5) for a 3 micron wide line [57].

$$j_n = -\frac{D_1}{gkT}\left(\sigma_{n-1} - \sigma_n\right) \tag{2.25}$$

where D_1 is the self-diffusion coefficient in bulk, and σ_n is the normal stress component in the longitudinal direction at the n*th* grain boundary. The grain boundary thickening rate for the n*th* grain boundary due to the mass conservation at the n*th* grain boundary is then given by

$$\frac{d\delta n}{dt} = \Omega(j_n - j_{n+1}) \tag{2.26}$$

The void volume can then be calculated for this model modifying equation (2.19), to give

$$V(t) = 2\Omega S \int_0^t J_1 dt = \frac{2\Omega SD}{kTg} \int_0^t \left(\sigma_0 - \Delta\sigma_1\right) dt \tag{2.27}$$

If only a single grain boundary on each side of the connecting grain boundary exists, then V(t) is given by

$$V(t) = 2V_r\left[1 - \exp(-t/\tau_0)\right] \tag{2.28}$$

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where $\tau_0 = \frac{g^2 kT}{M\Omega D_1}$ and V_r is the volume change per grain when the original strain is in the length of the direction is fully relaxed. Based on this model, the void volume is not a function of the grain boundary diffusion, but of bulk diffusion. For $t/\tau_0 < 10$, the model shows continuous growth for an infinitely long line with infinite grain boundaries, and for $t/\tau_0 = 2-3$, the saturation of growth for a one-grain boundary line.

McPherson and Dunn developed a model for void formation based on a power-law creep [19]. First, the model assumes that the elemental unit of failure is a vacancy. The transport of these vacancies into or out of a given region of interest is assumed to follow Fick's law, given by

$$J(y,t) = mn(y,t)F - D\frac{\partial n(y,t)}{\partial y} \tag{2.29}$$

where J is the vacancy flux, m is the mobility, n is the concentration of vacancies, F the average force acting on the vacancy, and D the diffusion coefficient for vacancies. In equation (2.29), the first term on the right is due to drift transport because of the force (stress gradient) acting on the vacancy, while the second term is associated with "back diffusion" due to a concentration gradient. If the force acting on the vacancy is proportional to the tensile stress σ, then equation (2.29) can be rewritten;

$$J(y,t) = D\left[1 - \frac{\partial n(y,t)/\partial y}{\beta n(y,t)\sigma}\right]\beta n(x,t)\sigma = \Phi(y,t)\exp\left[-Q/K_bT\right] \tag{2.30}$$

where β is a temperature dependent proportionality constant, and the Einstein relationship $m = D/kT = D_0\exp(-Q/kT)/kT$ was used. The model assumes that the drift component is much larger than the back diffusion component such that Φ is approximately independent of the stress. Failure will occur if a flux divergence exits, which is given as

$$\nabla \cdot J(x,t) = -\frac{\partial n(x,t)}{\partial t} \tag{2.31}$$

Using the divergence theorem, the integral form of Fick's law becomes

$$\int J \cdot dA = -\frac{dN(t)}{dt} \tag{2.32}$$

where A is the area of the surface bounding the volume of interest, and N(t) the total number of vacancies in the volume.

With the flux divergence equation established, the time-to-failure can be derived by first looking at the rate at which the number of vacancies increases in a given observation volume, given by:

$$\frac{dN_{vac}}{dt} = -\frac{dN_{ion}}{dt} = \lambda(t) N_{ion}(t) \qquad (2.33)$$

Here, N_{vac} and N_{ion} represent the number of vacancies and ions respectively, and $\lambda(t)$ is the metal-ion-emission probability per unit time. From equations (2.32) and (2.33), $\lambda(t)$ can be expressed as

$$\lambda(t) = \frac{\int J \cdot dA}{N(t)} \qquad (2.34)$$

If the number of Al ions in a given volume decreases to some critical factor f_c, failure will occur at time t when t=TF (Time to failure). Thus the critical factor is given by;

$$f_c = \frac{N(t = \mathrm{T}F)}{N_0} = \exp\left(-\langle\lambda\rangle TF\right) \qquad (2.35)$$

where $\langle\lambda\rangle$ is the time-averaged emission probability per unit time defined as;

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$$\langle \lambda \rangle = \frac{\int_0^{TF} \lambda(t)dt}{\int_0^{TF} dt} \tag{2.36}$$

By combining equations (2.34) through (2.36), the equation for TF can be determined, which is given by

$$TF = B_0 \sigma^{-1} \exp\left(\frac{Q}{kT}\right) \tag{2.37}$$

where B_0 in equation (2.37) is given by

$$B_0 = \frac{\ln(1/f_c)}{\langle [\Phi(b,t) - \Phi(a,t)] A_0 / N(t) \rangle} \tag{2.38}$$

For failure to occur, a flux divergence term must be present in the above equation. However, its impact on the time-to-failure is contained in the pre-factor B_0, and is not associated with the kinetics of failure. The generalized form of equation (2.37) is given as:

$$TF = B_0 \sigma^{-N} \exp\left(\frac{Q}{kT}\right) \tag{2.37}$$

Since the model developed by McPherson and Dunn is a model based on power-creep law, the above equation can be express as a creep rate (R) equation;

$$R = C(T - T_0)^N \exp\left(\frac{Q}{kT}\right) \tag{2.37}$$

where C is a constant, and T_0 is the temperature at which the stress is zero. The consequences of the above equation are shown in Fig. 2.7 where a maximum voiding rate can be found at an intermediate temperature.

The models so far presented have been developed for Al and void formation through grain boundary diffusion. However, in order to understand SIV in Cu interconnects, we will now discuss reported experimental, simulation, and modeling results by Singh *et. al.* [68]. Gan *et. al.* [46], and Huang *et. al.* [69]. These reports investigated the diffusion mechanisms that are responsible for stress relaxation, which in turn directly impact SIV behavior.

Singh *et. al.* [68] studied the stress relaxation in Cu interconnect structures by interface diffusion, through experiments and simulations. The authors measured the decrease in stress observed at elevated temperatures (Fig. 2.14), and then correlated

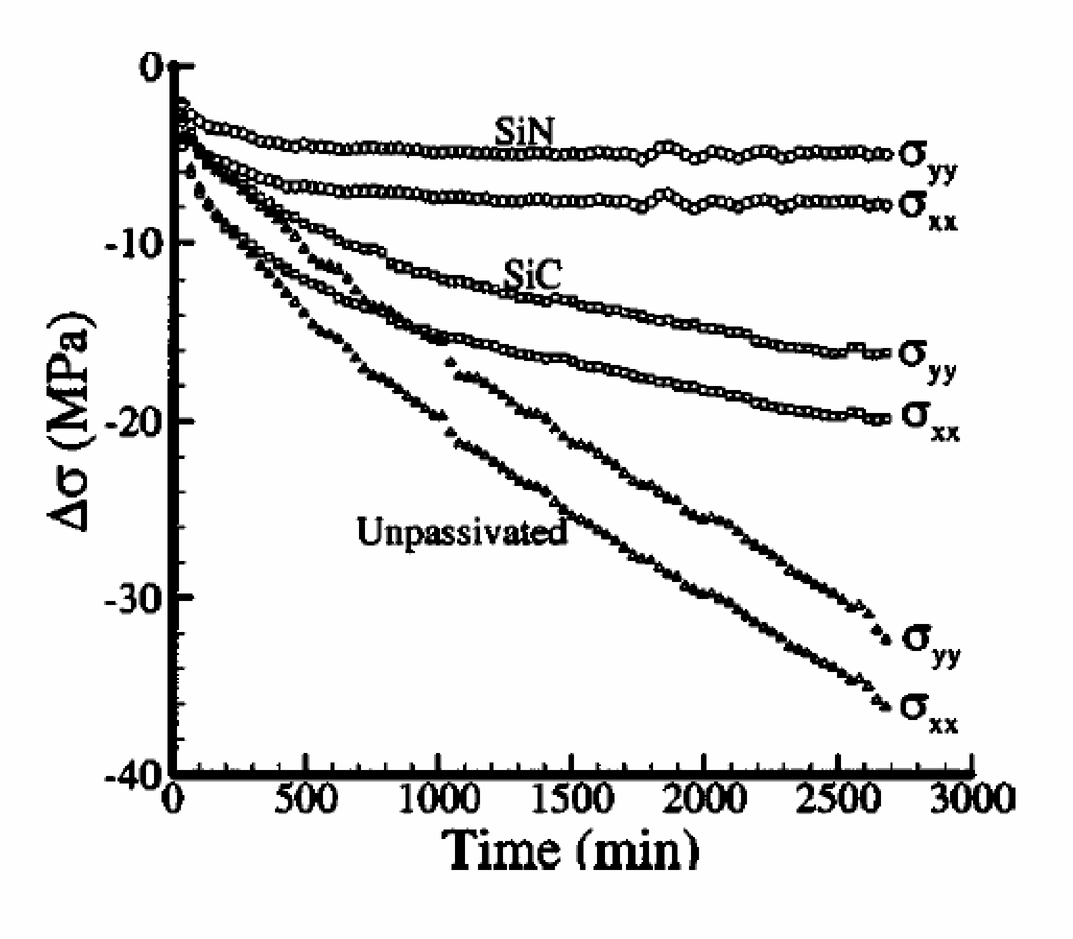

Fig. 2.14: Measured stress relaxation in an array of damascene copper lines. The results are shown for films passivated with SIN and SiC, as well as for unpassivated lines. σ_{xx} and σ_{yy} correspond to the normal stress along the length and transverse direction respectively [68].

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the possible diffusion paths responsible for the drop in stress. Two capping layers, SiN and SiC were used, and the results showed that if the Cu/cap interface diffusivity was constant, the difference in the elastic modulus between SiN and SiC did not affect the stress relaxation behavior. The authors concluded that in fact it was the difference in diffusivity at the interface, which was primarily responsible for the stress relaxation behavior. In the case of the two capping layers used, the slower diffusivity of SiN compared to SiC is believed to be the reason why the stress relaxation was slower in SiN than SiC (Fig. 2.14). The report also studied the diffusivity of Cu grain boundaries and Cu/Ta interface. Due to the strong adhesion of Cu/Ta, the diffusivity at this interface was much slower. In fact, an analysis of the data obtained showed the flux of the Cu/Ta interface to be approximately $D_{Cu/Ta}\delta_{Cu/Ta}\exp\left(-\frac{Q_{Cu/Ta}}{kT}\right) = 6.72\times10^{-31} m^3/s$ where $D_{Cu/Ta}$, $\delta_{Cu/Ta}$, and $Q_{Cu/Ta}$ are the diffusion coefficient, interface width, and the activation energy for diffusion at the Cu/Ta interface. This slow diffusivity at the Cu/Ta interface indicates that stress relaxation in Cu interconnects occurred by a flux of atoms from the Cu/passivation interface into the bamboo grain boundaries.

Gan et. al. [46] and Huang et. al. [69] studied experimentally the isothermal stress relaxation in electroplated Cu films, and presented kinetic models to explain the stress relaxation behavior. This study, which is composed of parts I [46] and II [69], found that a 1.0 micron thick Cu film passivated with a 50 nm SiN and 200 nm silicon oxide was less able to relax the stresses than an unpassivated Cu film, due to the faster surface diffusion available along the free surface of the unpassivated Cu film. Since the stress is related to the strain by the Hooke’s law, the stress rate can be expressed in terms of the strain rate by

$$\dot{\sigma} = -M\dot{\varepsilon}_p \tag{2.38}$$

where $\dot{\sigma}$ and $\dot{\varepsilon}_p$ are the stress rate and the inelastic strain rate, and M the biaxial modulus of the film. M was calculated to be $M=166.3-0.094T+7.59\times10^{-5}\ T^2$, where T is the temperature in ^{o}C. Assuming a linear creep behavior to be the chief mechanism for stress relaxation, the strain rate can be expressed as a linear creep, given by

$$\dot{\varepsilon}_p = \frac{\sigma}{\eta} \tag{2.39}$$

where η is the creep viscosity. The stress as a function of time can be calculated by inserting in equation (2.39) to (2.38), which gives

$$\sigma(t) = \sigma_0 \exp(-t/\tau) \tag{2.40}$$

where $\tau = \eta / M$ is a time constant of stress relaxation and σ_0 is the initial stress. This equation predicts that when $t = \tau$, full relaxation occurs (i.e. $\sigma(t) = 0$). However, experimental results show that this is not the case, and that the stress relaxation slows down as it nears the zero creep state. If this is taken into account, the empirical relation used to describe the stress relaxation behavior can be given by

$$\sigma(t) = \Delta\sigma_1 \exp(-t/\tau_1) + \Delta\sigma_2 \exp(-t/\tau_2) + \sigma_\infty \tag{2.41}$$

The two exponential terms represent the stress relaxation from the steady state and transient states, while σ_∞ is the zero creep stress. In order to be able to consistently apply equation (2.41) to conditions with varying parameters, a subsequent kinetic model was developed.

The kinetic model presented by Huang [69] looks at the diffusion paths by which mass transport occurs (free surface, grain boundary, Cu/cap interface) (Fig. 2.15). In this paper, bulk diffusion and Cu/substrate diffusion is neglected. Neglecting the Cu/substrate diffusion does not seem unrealistic given the fact that the Cu/diffusion barrier has low diffusivity, as was discussed earlier. The chemical potential is defined by the local grain curvature at the free surface and the normal stresses at the grain boundaries. This chemical potential gradient is the driving force behind the diffusion that relaxes the stress in the metal layers. First the stress relaxation of a free Cu

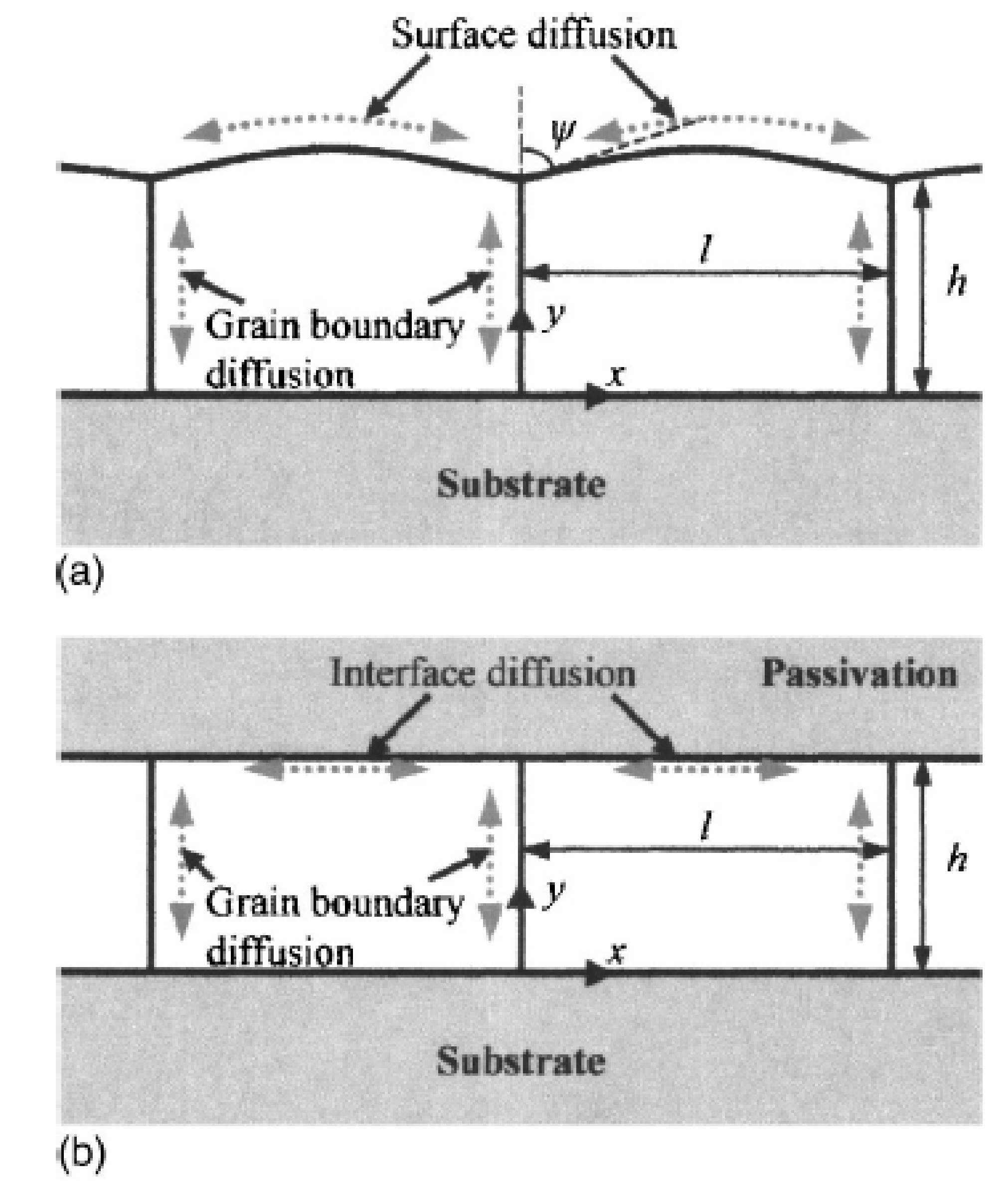


Fig. 2.15: Schematic illustration of polycrystalline thin films; (a) an unpassivated film and (b) a passivated film [68].

surface was considered. The kinetic model assumed a film consisting of two-dimensional grains of a constant length l with grain boundaries of height h perpendicular to the film/substrate interface (Fig. 2.15). The chemical potential driving the diffusion at the free surface and the grain boundary is given by

$$\mu_S = \mu_0 - \kappa(S)\gamma_S\Omega \qquad (2.42)$$

$$\mu_B = \mu_0 - \sigma_B(S)\gamma_S\Omega \qquad (2.43)$$

where μ_0 is the reference value, γ_S the surface energy density, Ω the atomic volume, and κ the surface curvature. σ_B is the normal stress at the grain boundary, y is the coordinate along the grain boundary, and s is the curvilinear coordinate along the surface. Under equilibrium conditions, no chemical potential gradient exists, and no driving force for diffusion exists. In addition, the curvature of the free surface grains is uniform ($\kappa(S) = \kappa_0$), and the normal stress at each grain boundary is a constant ($\sigma_B(y) = \sigma_{B0}$).The equilibrium conditions can be derived from simple geometric considerations where

$$\kappa_0 = -\frac{2\cos\psi}{l} \qquad (2.44)$$

Since the surface energies and the grain boundary energies at equilibrium form a relationship where $2\gamma_s \cos\psi = \gamma_B$ (γ_B is the grain boundary energy density). From the above, the continuity of the chemical potential at the free surface and grain boundary requires that

$$\sigma_{B0} = \kappa_0 \gamma_S \tag{2.45}$$

The effective stress of the film is given by

$$\sigma_f = \frac{1}{h}\int_0^h \sigma_B(y)dy + \frac{\gamma_S}{h}\sin\psi \tag{2.46}$$

where the first term is the average of the normal stress along the grain boundary, while the second term represents the in-plane component of the surface tension.

The residual film stress at the equilibrium state can then be calculated by inserting (2.45) into (2.46) giving

$$\sigma_{FQ} = \frac{\gamma_S}{h}\left(\kappa_0 h + \sin\psi\right) \tag{2.47}$$

Since this is the stress at which equilibrium is achieved, no chemical potential gradient exists, and diffusional creep stops. This is called zero-creep stress.

In order to calculate the variation of effective stress as a function of time, we need to determine the first term in equation (2.46). This can be done by looking into equation (2.15). To be consistent with the notation of Huang *et. al.* [69], equation (2.15) is rewritten as

$$\frac{d\sigma_B}{dt} = \frac{M\Omega\delta_B D_B}{lkT}\frac{d^2\sigma}{dy^2} \tag{2.48}$$

This is a standard diffusion equation in terms of the grain boundary stress. In order to solve this equation for the grain boundary stress, the boundary conditions $\left.\frac{\partial\sigma_B}{\partial y}\right|_{y=0} = 0$ (no atomic flux at the root of the grain boundary) and $\sigma_B(y = h) = \kappa_0\gamma_S$ (continuity equation assuming infinitely fast surface diffusion are assumed. This gives the effective stress at t=0:

$$\sigma_B(t = 0) = \kappa_0\gamma_S + \sum_{n=0}^{\infty} A_n \cos(k_n y)\exp(-\overline{D}_B k_n^2 t) \tag{2.49}$$

where $\overline{D}_B = M\Omega\delta_B D_B / kT$ and $k_n = [(2n+1)\pi / 2h]$. If it is assumed that initially the grain boundary stress is uniform and the effective film stress is σ_0, then equation

(2.46) becomes

$$\sigma_B(t=0) = \sigma_0 - \frac{\gamma_s}{h}\sin\psi \tag{2.50}$$

Inserting this initial grain boundary stress to equation (2.49) gives the solution for A_n in equation (2.49), in the form

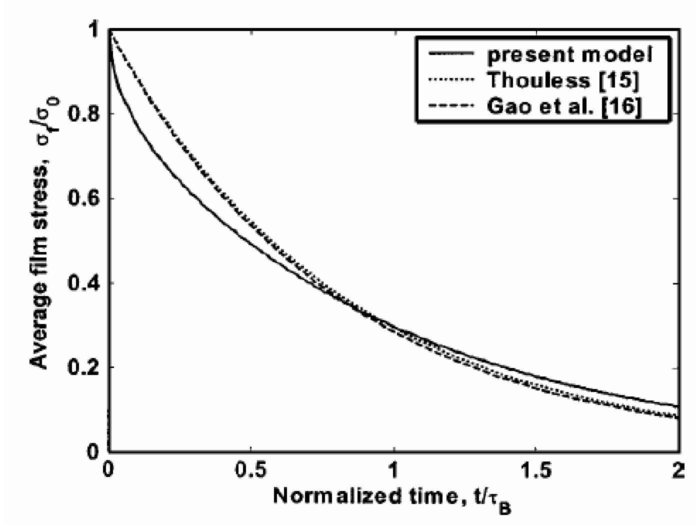
$$A_n = \frac{(-1)^n}{2n+1}\frac{4}{\pi}\left(\sigma_0 - \sigma_{EQ}\right) \tag{2.51}$$

Substituting equation (2.49) into equation (2.46) leads to the effective film stress as a function of time given by

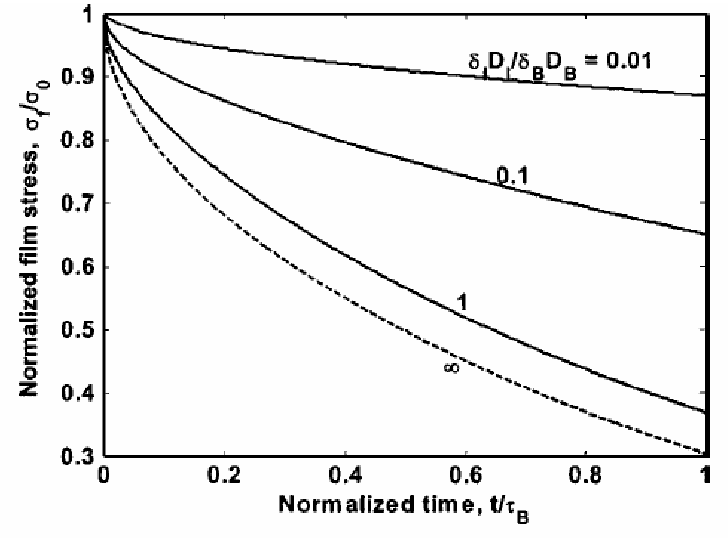
$$\sigma_f(t) = \sigma_{EQ} + (\sigma_0 - \sigma_{EQ})\frac{8}{\pi^2}\sum_{n=0}^{\infty}\frac{\exp(-\overline{D}_B k_n^2 t)}{(2n+1)^2} \tag{2.52}$$

This equation describes the stress relaxation under isothermal conditions, showing that stresses decrease quickly at first, but then a decrease in the stress relaxation rate is observed (Fig. 2.16 (a)).

In case of the passivated film, Huang *et. al.* [69] assumed that atoms diffuse along



(a)



(b)

Fig. 2.16: (a) Stress relaxation for an unpassivated film and (b) for a passivated film predicted by Huang et. al. [69].

the grain boundary and the interface between the film and the passivation layer. Another assumption made is that the Cu/cap layer interface is flat, and that the mass transport induces a locally nonzero stress at the grain boundaries ($\sigma_I(t)$), similar to the normal stress at the grain boundaries. When diffusion at the Cu/cap layer interface occurs, the matter transported due to the divergence of atomic flux can be accommodated by the interface by either deformation of the grains, or a rigid body motion of the passivation layer. The model assumes elastic grains and a rigid passivation layer, and the local normal stress associated with the elastic deformation is given as

$$\frac{\partial \sigma_I}{\partial t} = \frac{M}{h}\left[\Omega \frac{\partial J_I}{\partial x} + \Delta(t)\right] \tag{2.53}$$

where $\Delta(t)$ is the displacement of the passivation layer perpendicular to the interface, assumed to be uniform for a rigid layer passivation. For $\sigma_I(t)$, the total normal stress at the interface must be zero for mechanical equilibrium and thus,

$$\int_0^{l/2} \sigma_I(x) = 0 \tag{2.54}$$

Since the chemical potential at the interface can be derived in a way similar to that for the grain boundary (equation (2.43)), we can write

$$\mu_I = \mu_0 - \sigma_I(x)\Omega \qquad (2.55)$$

Modifying the equation for flux for the case of interfacial diffusion gives

$$J_I = -\frac{\delta_I D_I}{\Omega kT}\frac{\partial \mu_I}{\partial x} \qquad (2.56)$$

Combining equations (2.53) through (2.56) gives

$$\frac{\partial \sigma_I}{\partial t} = \frac{M\Omega\delta_I D_I}{hkT}\left[\frac{\partial^2 \sigma_I}{\partial x^2} + \frac{M}{h}\Delta(t)\right] \qquad (2.57)$$

In order to derive $\sigma_I(x,t)$, the following boundary conditions were assumed, namely no flux at x=l/2, and ensuring continuity of flux and chemical potential at the junction between the interface and a grain boundary. From the boundary conditions, the solution for $\sigma_I(x,t)$ can be obtained for the passivated Cu films;

$$\sigma_I(x,t) = \sigma_B(t) + \sum_{n=0}^{\infty} A_n \sin(k_n x)\exp(-\overline{D}_I k_n^2 t) \qquad (2.58)$$

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where;

$$\overline{D}_I = \frac{M\Omega\delta_I D_I}{hkT} \tag{2.59}$$

$$k_n l = (2n+1)\pi \tag{2.60}$$

$$A_n = -\frac{4\sigma_0}{(2n+1)\pi} \tag{2.61}$$

$$\sigma_B(t) = \sigma_0 \frac{8}{\pi^2} \sum_{n=0}^{\infty} \frac{\exp(-\overline{D}_I k_n^2 t)}{(2n+1)^2} \tag{2.62}$$

Equations (2.49) and (2.62) each give the stress as a function of time for the case of an unpassivated, and passivated film respectively. The change in stress as a function of time for the models discussed in [69] is shown in Fig. 2.16 (a) and (b). In Fig. 2.16 (b), the ratio of the interface to grain boundary diffusion ratio is shown. The results show that the diffusivity for the passivated case is very sensitive to the diffusivity of the interface diffusion. Since it is generally understood that the diffusion at the grain boundary is faster than the interface diffusion, the interface diffusion is expected to have a large impact on the stress relaxation behavior. Fig. 2.17 (a) and (b) shows the calculated diffusivity at the grain boundary and the interface from this work.

In addition to the above SIV models [29, 30], several experimental results describing SIV in detail have also been presented [20,27,59,64-67]. Some of the

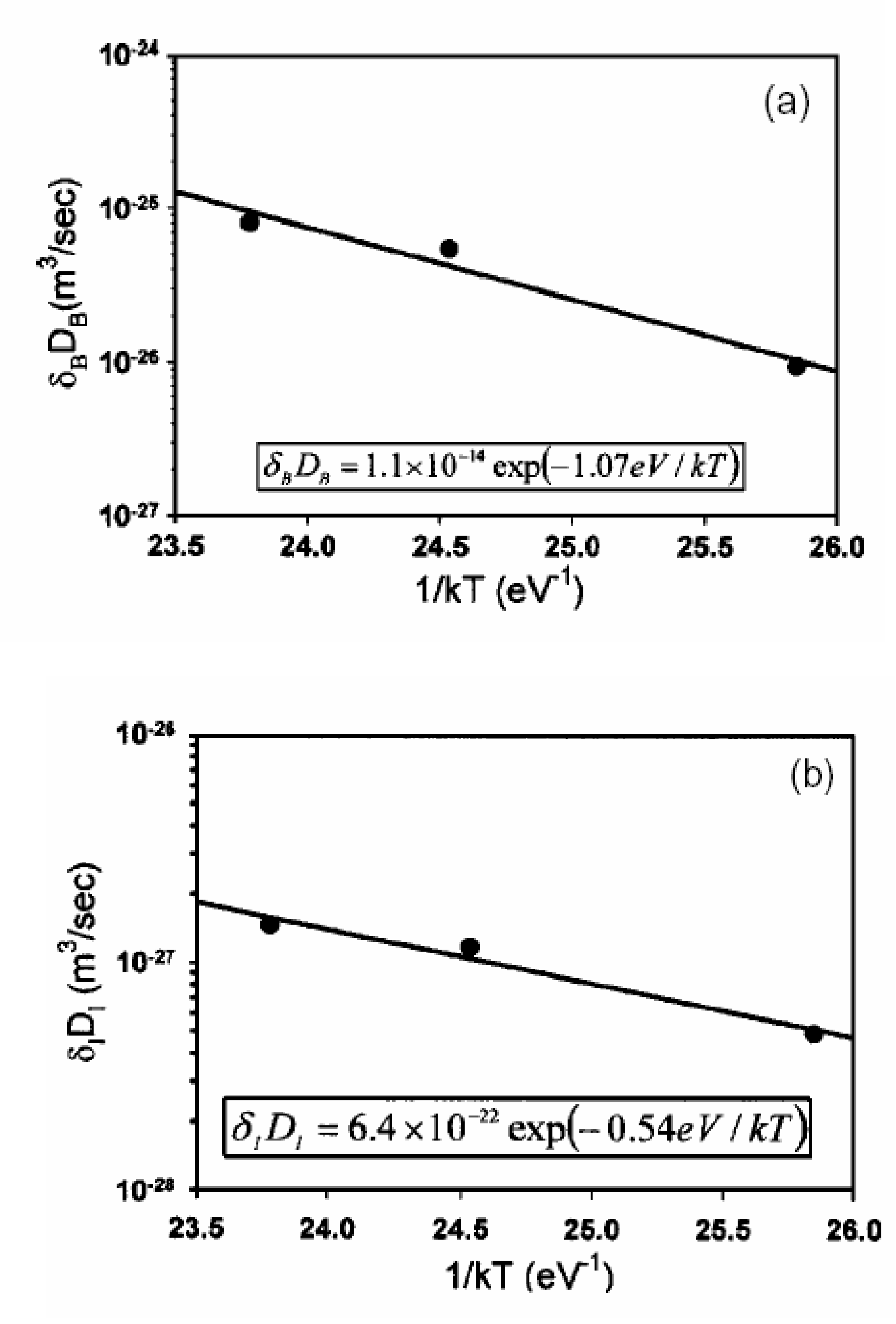


Fig. 2.17: Calculated diffusion coefficients for (a) grain boundary and (b) interface [46]

experiments have tried to correlate void formation sites with crystal orientation/local stresses. For Al, in most cases, void growth occurred by the exposure of low energy {111} type surfaces [59]. In addition, voids had a tendency to open up on grain orientations with high energy, such as {233} or {122} grains. Thus, in the case of Al, voids occur on grains with high surface energies, by exposing lower surface {111} planes (Fig. 2.18). As the voids continue to grow, the voids form a characteristic angle, which at equilibrium is given by (2.7) [27].

$$E_g = 2E_s \cos(\theta / 2) \tag{2.62}$$

In addition, reports were presented on the nucleation and local texture behavior of Cu interconnects [65-67], which showed {111} textures to have better resistance to SIV, similar to EM. Furthermore, Nucci *et. al.* [66] reported that when voids did form at {111} grains, these grains were typically a few degrees from the {111} zone axis, in contrast to strong {111} textured grains where voiding did not seem to occur. A look at the misorientation angle ($>10^o$) also elucidated the role of grain boundaries, where higher misorientation angles led to higher fraction of voids. According to [65], this was due to the fact that higher misorientation angles leads to higher grain boundary energy, and as a result, the critical free energy change for void formation decreases with increasing misorientation angle.

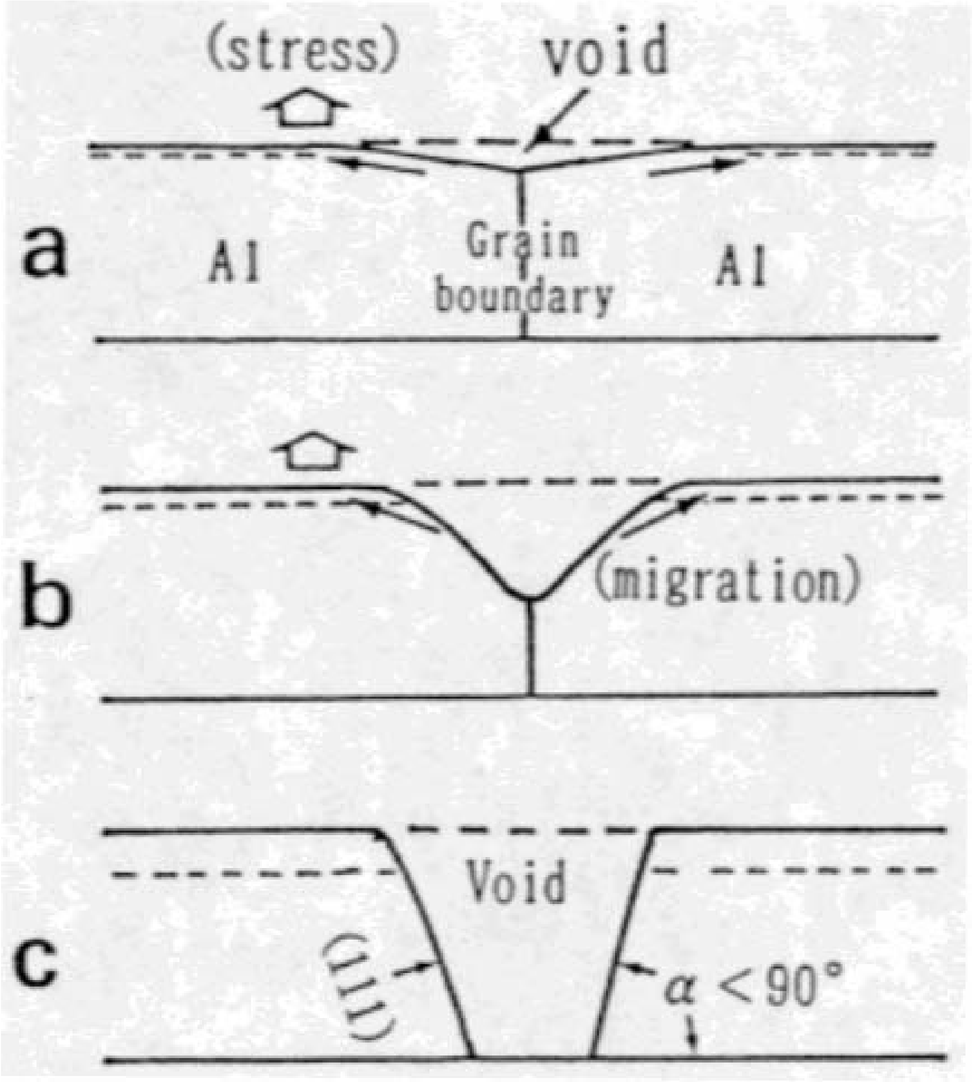


Fig. 2.18: Void opening a low surface energy {111} in an Al line [59].

2.4 GRAIN ORIENTATION IN CU INTERCONNECTS

Cu thin films can be deposited onto a substrate by different methods, including chemical vapor deposition (CVD), physical vapor deposition (PVD), and electroplating. The resulting texture of these Cu thin films depends on the deposition process. In particular, PVD produces a strong (111) texture, CVD a random texture [71], whereas electroplating results in a (111) texture [72]. As the electroplating method is currently used for the fabrication of Cu for interconnects, the texture in these thin films has been extensively studied [72-76].

Cu interconnects are fabricated by the damascene process, which involves first depositing an ILD (interlayer dielectric) layer, followed by etching the ILD to form trenches. Subsequently, the Cu metal is deposited by electroplating, and planarized by Chemical Mechanical Polishing (CMP), before another layer of ILD is deposited on top (Fig. 2.19). Because the Cu material is deposited into etched trenches, the texture of electroplated Cu interconnects is more complex than for thin films. For wide lines, the texture is dominated by grains growing from the bottom of the trench. However, as the Cu interconnect linewidth decreases, the texture of the lines is greatly influenced by sidewall grain growth (Fig. 2.20) [73].

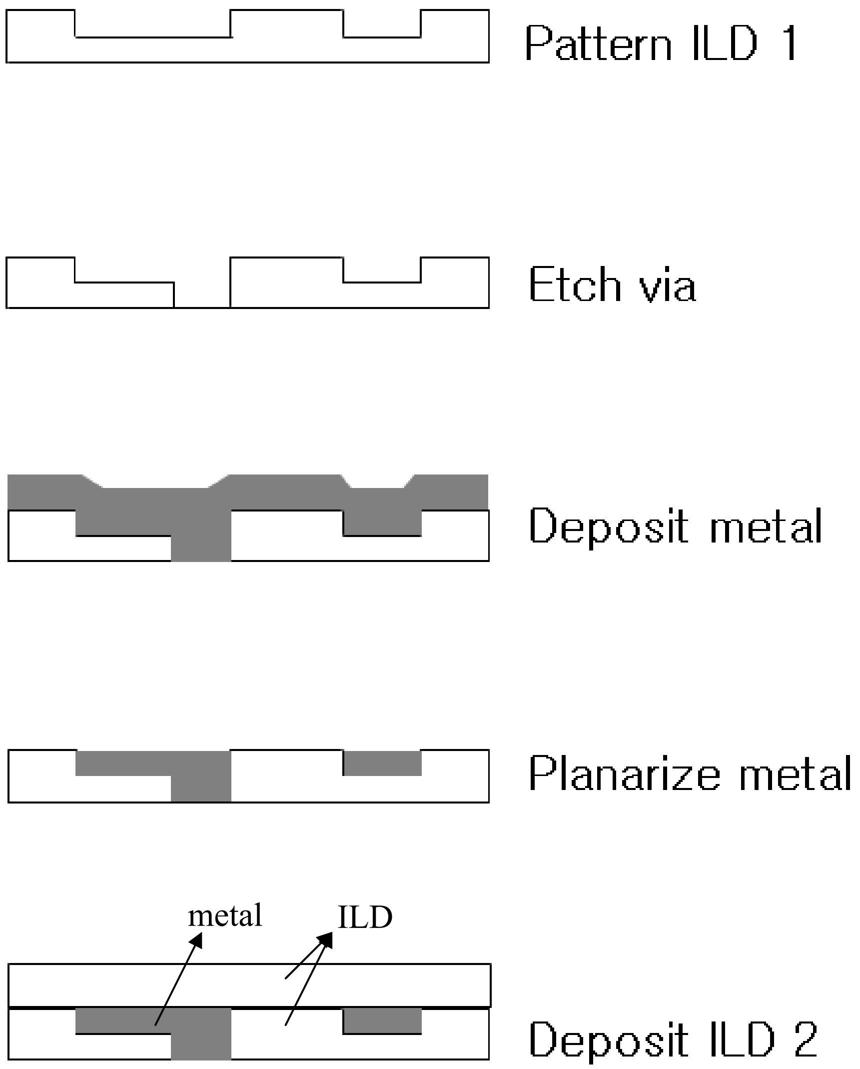
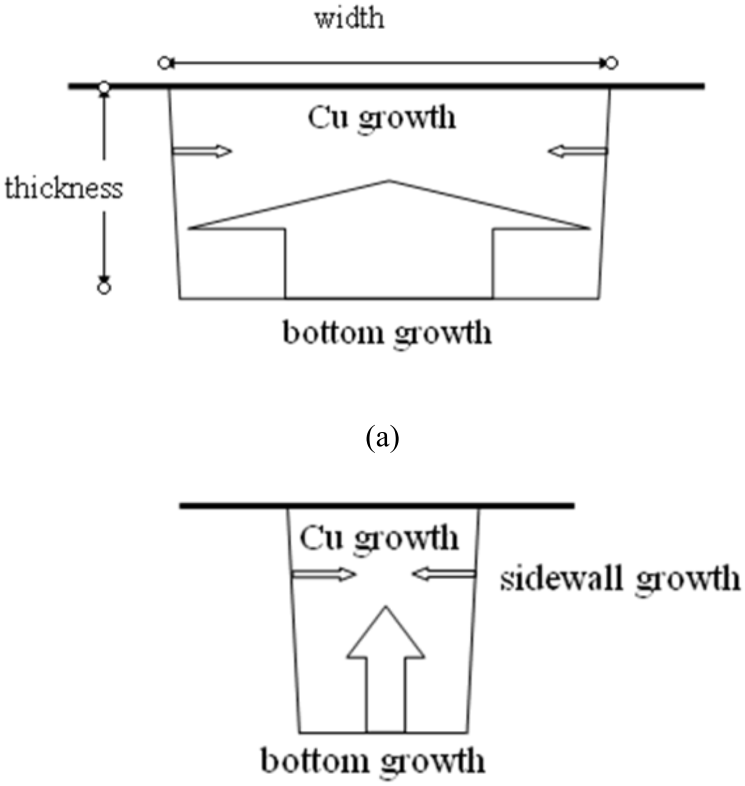


Fig. 2.19: Damascene fabrication process for depositing Cu [77].



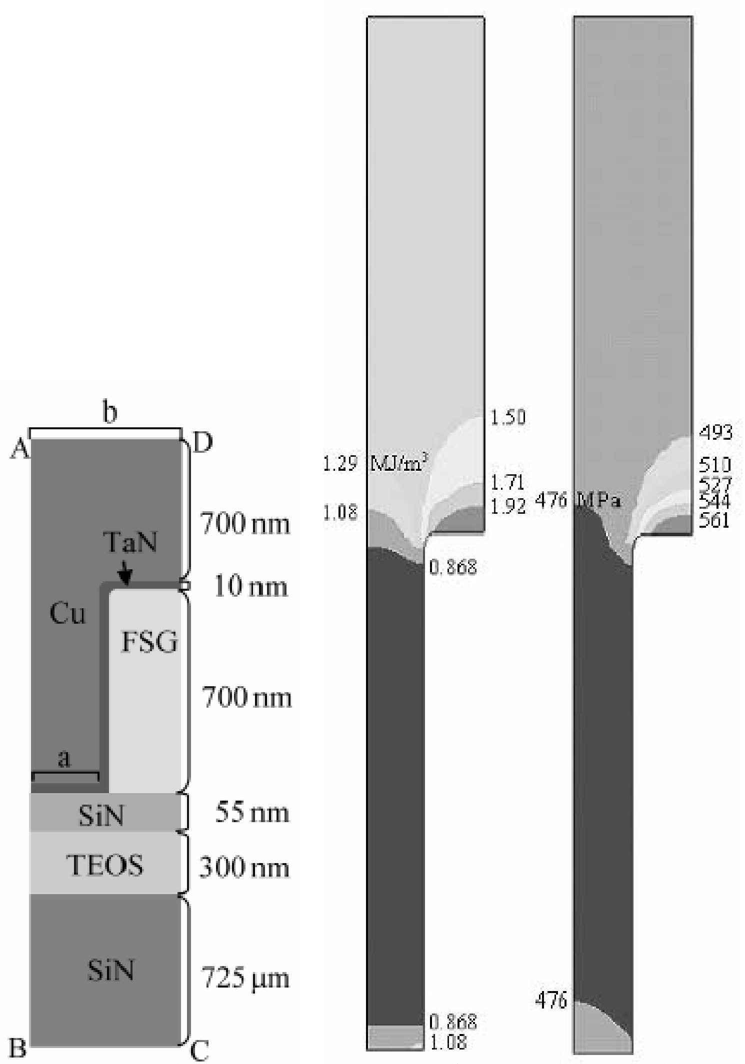
(a)

(b)

Fig. 2.20: (a) Cu deposition of wide lines-strong bottom growth (b) Cu deposition of narrow lines-strong sidewall growth [56].

Electron Back Scattered Diffraction (EBSD) analysis of Cu interconnects has shown that the texture is typically {111}<110>//RD (Rolling Direction along the length of the lines) for linewidths ranging from 1.0 microns to 0.14 microns [75]. Similar findings have also been reported for Cu lines less than 2 microns in width [73,76]. In addition to the {111}<110>//RD textured grains, Cho *et. al.* [73] also showed that {115} type textures develop in Cu during annealing of the electroplated Cu. However, due to the resolution limitations of EBSD, many small grains, especially in the 0.14 micron wide lines, were not indexed, limiting significantly the overall analysis. Since narrower lines result in stronger sidewall textures, a more detailed look should provide further insight into the texture of Cu interconnects. This will be discussed later in the dissertation

The reason for the strong {111}<110>//RD orientation has been suggested by Lee *et. al.* [76] and Cho *et. al.* 73], who claimed that 1) the strain energy distribution is highest at the upper corner of the trench (Fig. 2.21), and 2) due to the high anisotropy of the Cu, the grains will try to align along the crystallographic direction which will minimize the strain energy. As the lowest elastic modulus for Cu is in the [100] direction (Fig. 2.22), the Cu grains will try to align the [100] direction along the upper corner of the trench with the maximum stress direction (MSD). However on the (111) plane, there are no <100> directions available. As a result, the textured (111) Cu grains will align along the [112] direction, which is the closest available low-indexed direction to the [100] direction (35.3^o apart) (Fig. 2.23).



(a) (b) (c)

Fig. 2.21: From left to right, (a) cross sectional structure of a damascene trench (b) strain energy distribution and (c) maximum principal stress distribution in Cu deposited in and over damascene trench with a=100 nm and b=200nm [76].

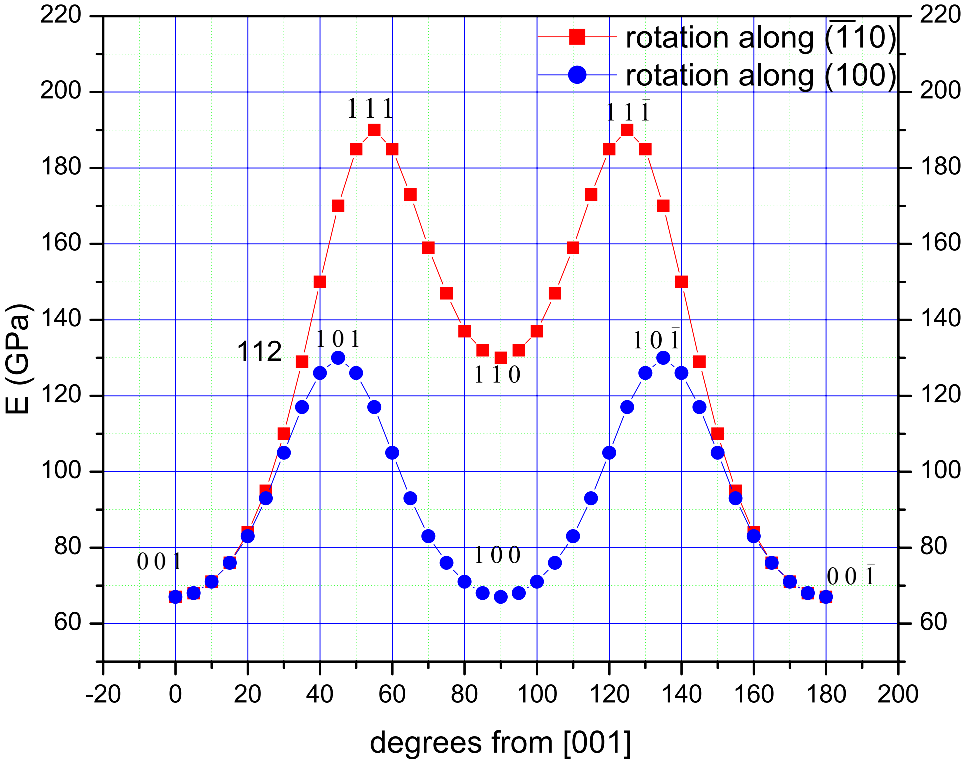


Fig. 2.22: Variation of Young's modulus in Cu as a function of crystal direction.

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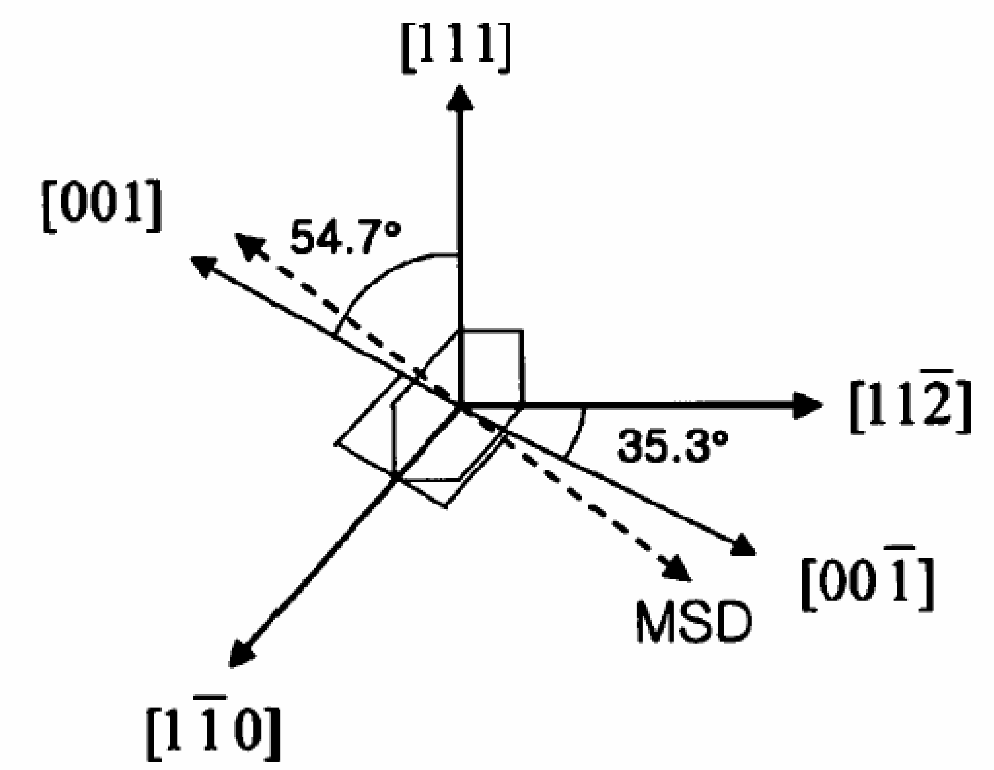
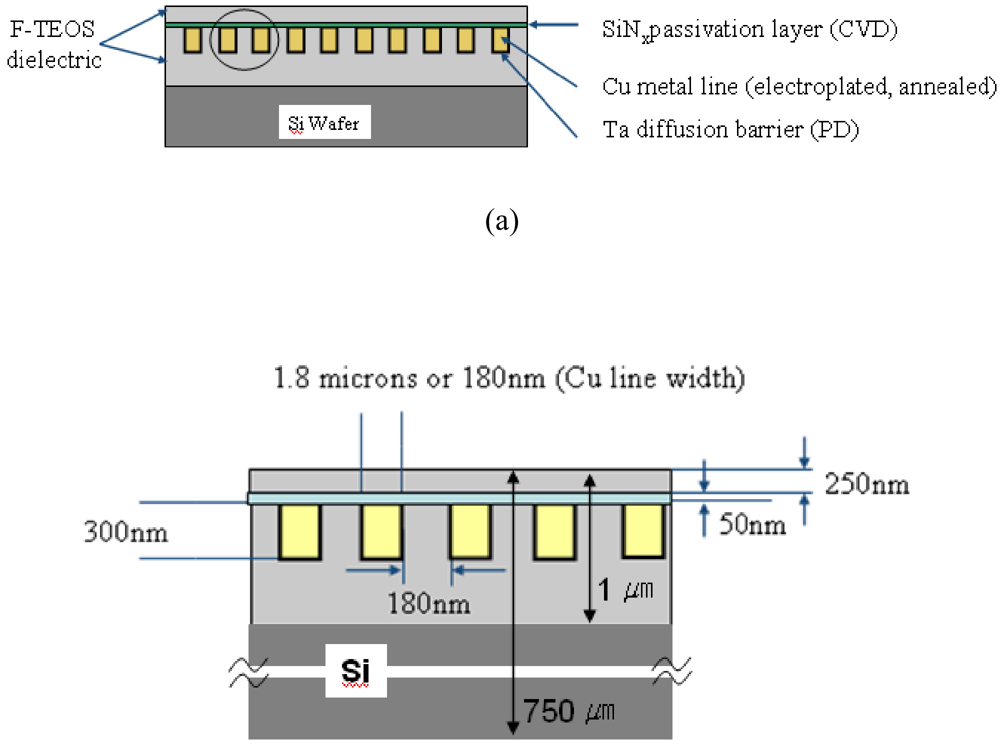


Fig. 2.23: Relationship among [111], $[\bar{1}10]$, $[11\bar{2}]$, and [001] direction. Maximum stress direction (MSD) and [111], [001], and $[11\bar{2}]$ direction are on sample plane [75].

CHAPTER 3: EXPERIMENTAL PROCEDURE

3.1 SAMPLE FABRICATION

The Cu interconnect samples were provided by Freescale Semiconductors. The as-received test structure consisted of electroplated damascene Cu lines integrated with interlayer dielectrics (ILD), Ta diffusion barrier (DB), and SiN_x passivation on a Si substrate (Fig. 3.1a). The Ta DB was physically deposited, while the SiN_x was deposited using chemical vapor deposition. The electroplated Cu lines were annealed at 250°C for 30 minutes to promote grain growth. The Cu lines used in this work were 1.8 microns and 180 nm wide with a thickness of 300 nm. The aspect ratio (thickness/width ratio) was 1.67 and 0.17 respectively, while the pitch was 1.98 microns and 0.36 microns respectively. The ILD material was F-doped SiO_2 (F-TEOS). The Ta diffusion barrier was 10-20 nm thick, and the SiN_x passivation was 50 nm thick. The thickness of the wafer was 750 μm (Fig. 3.1b).



(a)

(b)

Fig. 3. 1: (a) Schematic of Cu interconnect sample (b) Dimensions associated with each layer.

3.2 TEM SAMPLE PREPARATION

3.2.1 TEM sample preparation for planar view

Planar samples were prepared by a conventional TEM sample preparation method. The sample preparation consisted of disc cutting, mechanical polishing, dimpling and ion milling. A Fischione 150 Ultrasonic Disk Cutter was used to cut a 3 mm disc from the wafer (Fig. 3.2a), which was then mechanically polished using a diamond lapping film with grit sizes in order of 30, 15, 6, 3, 1, and 0.5 microns to a thickness of ~100 microns (Fig. 3.2b). The sample thickness during lapping was accurately controlled by using a Tripod Polisher^{TM}. The polished sample was dimpled to a thickness of ~4 microns (Fig. 3.2c) using a Fishione 150 Dimpling Grinder. The sample was then ion milled to electron transparent thickness with a Fishione 1010 Ion Miller (Fig. 3.2d) using conditions of 5.0 KeV/5.0 mA using a beam angle of 10^o. The ion miller is equipped with two ion guns, one on each side of the sample. As the Cu interconnect lines are at the top of the wafer with an approximate 300 nm of ILD and passivation layer, the samples were ion milled mostly from the bottom. The top layer was milled for only a few minutes at 3.0 KeV/3.0 mA to ensure that the top passivation layer was milled just enough so that the Cu/passivation layer interface was kept intact. This is important, as this interface plays a key role in the stress relaxation behavior of Cu interconnects.

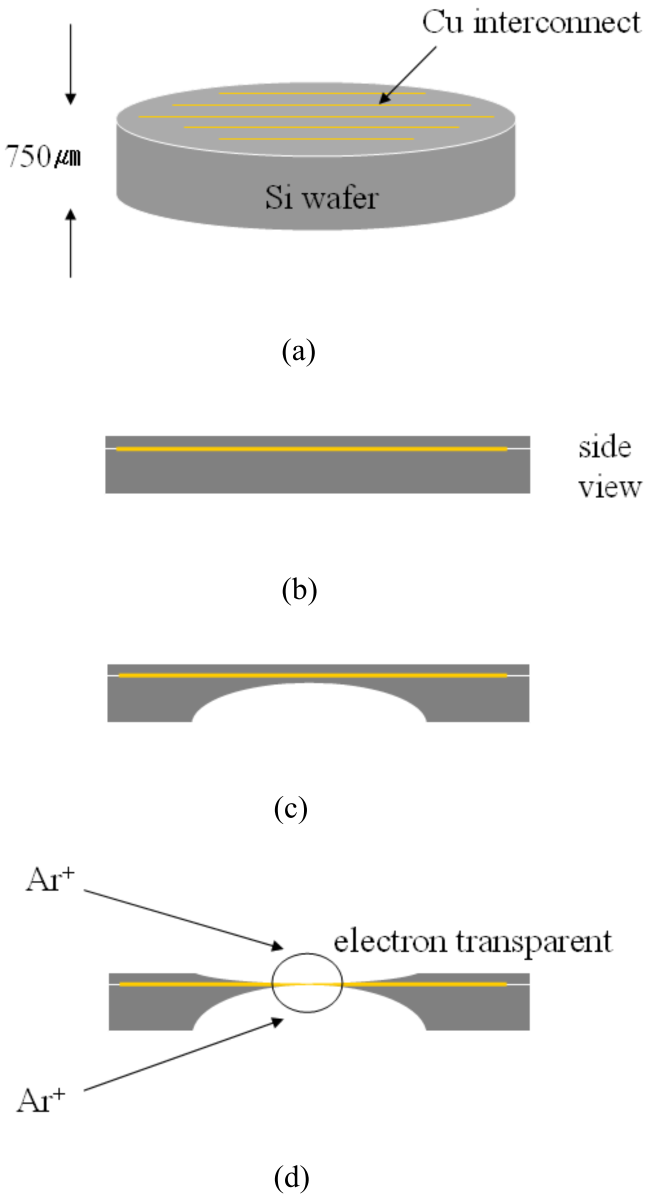


Fig. 3. 2: a) Disc cutting (3 mm diameter) b) Polishing (thickness <100microns) c) Dimple grinding (thickness ~4microns) d) Ion Milling

3.2.2 TEM sample preparation for cross section view

While the TEM sample preparation of planar specimens can be performed using conventional techniques, the fabrication of site specific cross-sectional samples are best produced with the use of a Focused Ion Beam (FIB) [78-79]. FIBs generally employ Ga as the beam source, which is used to sputter material away from the target substrate by rastering the Ga ions. This allows the FIB operator to fabricate TEM specimens precisely, down to below 100 nm in specimen thickness. Two FIB techniques have been widely used to fabricate TEM samples, the Liftout Technique and the Trench (H-Bar) Technique [79]. The Liftout Technique involves cutting a thin layer of the target material using the FIB, and then subsequently plucking the TEM sample onto a thin membrane, using a micromanipulator. However, using this procedure, only small samples (typically 5 microns in width) can be fabricated. This in turn, makes *in-situ* TEM heating experiments above 100^{o}C difficult to perform due to a lack of thermal stability of the membrane supporting the sample on the TEM grid.

For this reason, the trench technique was used to prepare TEM cross-sectional samples in a FEI Strata 235 Dual Beam FIB equipped with a Field Emission Gun (FEG). The FEI Strata 235 Dual Beam FIB is equipped with both an electron gun and an ion beam placed at a 52^{o} angle that allows the use of the electron gun to observe the milling process while the ion gun is in use (Fig. 3.3). The trench technique requires pre-thinning a 2.5 mm wide sample to ~100 microns in thickness. ‘Trenches’

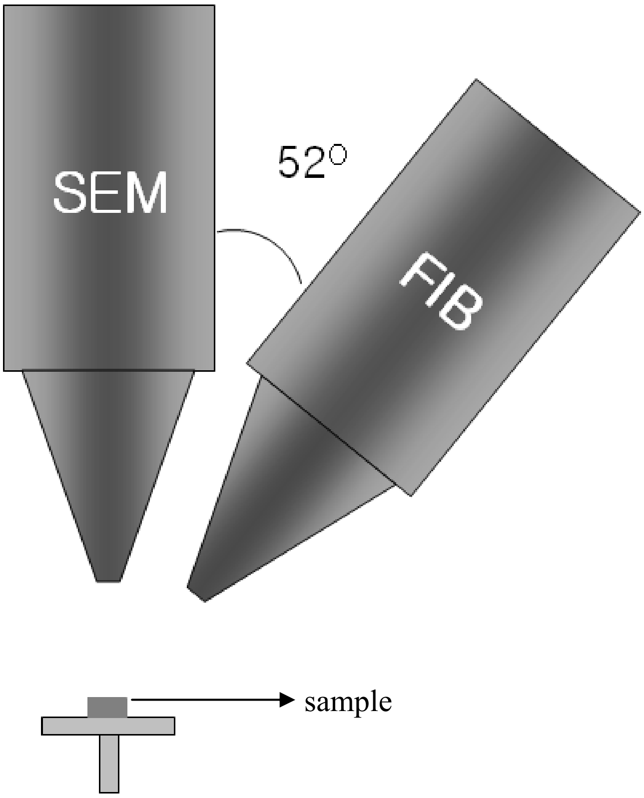
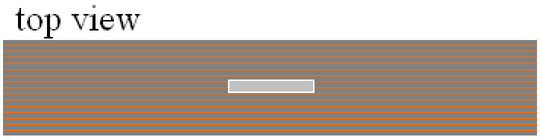


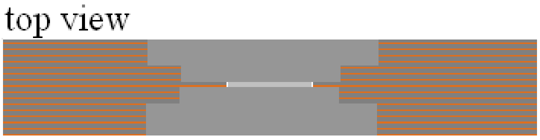
Fig. 3. 3: Schematic diagram of the dual beam FIB. The SEM and FIB guns are at an angle of 52^{O}.

were then milled using the Ga ion beam, leaving a thin TEM sample (Fig. 3.4). Final cleaning was done with a 30 keV/10 pA beam to minimize beam damage to target specimens. Figure 3.4d is an SEM image of one of the prepared TEM samples.

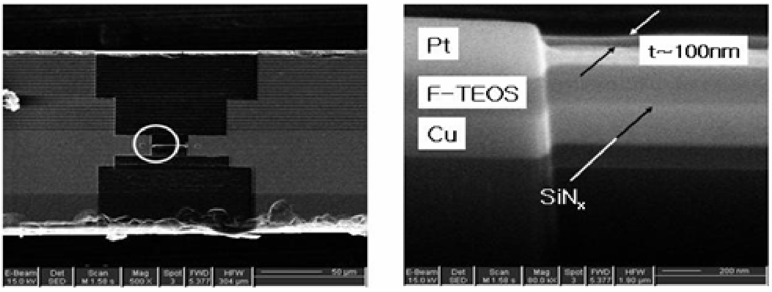
(a) Sectioning (dicing saw)
100 ㎛×2.5 mm



(b) Pt deposition on target area



(c) Use FIB to make TEM sample
(using Trench Technique)



(d) SEM image of TEM sample made with FIB

Fig. 3. 4: Schematic illustration of the FIB trench technique (a)-(c) and (d) SEM image of the prepared TEM sample via the trench technique.

3.3 STRESS CHANGES IN CU INTERCONNECTS DUE TO TEM SAMPLE PREPARATION

TEM observations of Cu interconnects require thinning a small portion of the sample to thicknesses below 100 nm. Such a procedure can affect the original state of stresses, especially in Cu interconnects. In order to assess such changes in stress due to TEM sample preparation, stress simulations were performed for the Cu interconnects lines investigated in this work. TEM sample thickness measurements and thickness profiles necessary for the Finite Element Method (FEM) calculations were done by the author, while FEM stress calculations were done by Haixia Mei in Professor Huang's research group in the Department of Aerospace Engineering, The University of Texas at Austin.

In order to obtain the thickness profile away from the electron transparent area a Veeco Profilometer was used. The thickness of the electron transparent area was measured using Kossel-Mollenstedt fringes in a Zero Order Laue Zone (ZOLZ) CBED pattern [80].

A multilayer model (Fig. 3.5), comprised from bottom up, by a dielectric layer (400 nm), a Cu film (300 nm), a SiN_x passivation layer (50 nm) and another dielectric layer (250 nm), with a total film thickness of 1 micron was considered for the stress calculations. Both the SiN_x passivation and dielectric layers were removed from the

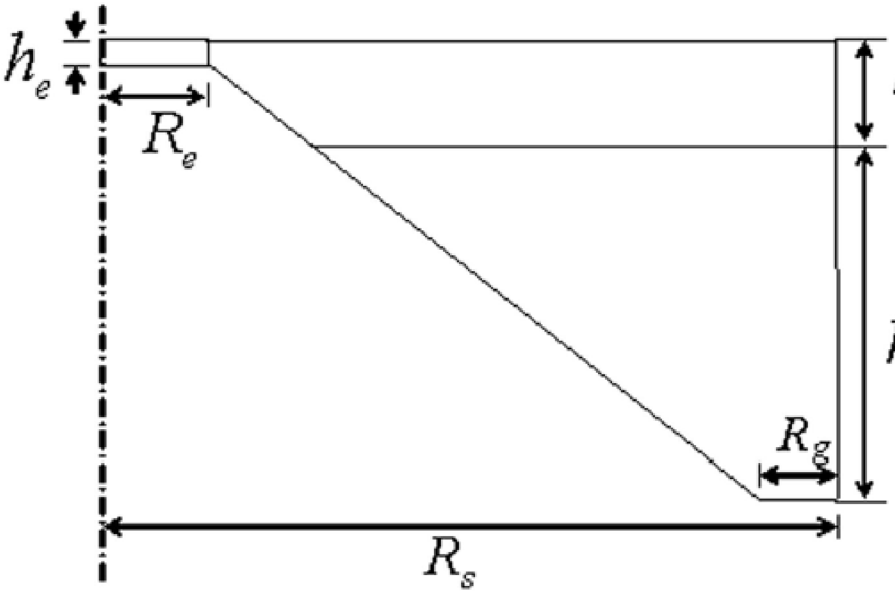


Fig. 3. 5: Schematic of the axisymmetric FEM model of the TEM specimen. h_f is the film thickness (multilayer), h_s the substrate thickness, R_s the wafer radius, h_e the electron transparent area thickness and R_e the electron transparent area radius.

center region of the specimens, leaving only Cu in the electron transparent area of the sample.

The stresses in the TEM specimens were calculated from an axisymmetric finite element model using the commercial package ABAQUS [81]. As illustrated in Fig. 3.5, the specimen is roller supported along its outer edge and subject to rotational symmetry at its central axis. A relatively fine FEM mesh was used for the film, especially for the electron transparent area. The material properties used in the FEM analysis are listed in Table 3.1.

Table 3.1: Mechanical properties used for Finite Element Analysis of TEM specimen [83].

	Young's modulus (GPa)	Poisson's ratio	CTE (ppm/K)
Si	165	0.22	4.2
Cu	128	0.36	17.0
TEOS	72	0.20	1.4
SiLK	2.45	0.35	66.0

3.4 *IN-SITU* TEM HEATING

In-situ TEM heating experiments were conducted in both a JEOL 200CX and a FEI TECNAI TEM, equipped with Gatan heating stages, in particular a single-tilt and a double-tilt stage for the JEOL 200CX and the FEI TECNAI TEM, respectively. A water recirculator was connected to the heating stage to minimize thermal drift during *in-situ* heating. Initial *in-situ* TEM heating of the Cu interconnect samples was conducted from room temperature to 500 ^{o}C at a rate of 10 ^{o}C/min. Subsequently, three thermal cycles were performed from 300 ^{o}C to 500 ^{o}C under heating and cooling rates of approximately 15 ^{o}C/min. In order to minimize the oxidation of the exposed Cu interconnects, the in-situ TEM heating was performed immediately following the TEM sample preparation, and a plasma cleaner was also used to remove any possible oxidation of the Cu post TEM sample preparation.

Live recording of the *in-situ* TEM experiments was done using a software called Camtasia Live by TECHSMITH. Videos were captured at speeds of 10-15 frames per second.

3.5 GRAING ORIENTATION ANALYSIS USING ACT

The local grain orientation of Cu interconnect lines was obtained by analysis of diffraction patterns (DP) taken in a JEOL 2010F TEM. Obtaining DP using the Select Area Diffraction (SAD) aperture can be difficult for very fine grains below a few tens of nanometers in size. Even with the smallest select area aperture, the beam is too large to obtain a DP from a grain 100 nm or less in diameter. Therefore, in order to obtain DP from individual grains, convergent beam diffraction (CBED) or Nano Beam Diffraction (NBD) must be used. To ensure that the DP is as focused as possible, so that the d-spacing can be accurately calculated for crystal orientation indexing, the smallest C2 condenser aperture was used (10 micron in this particular work). In this fashion, using the NBD mode, an electron beam probe only a few nanometers in diameter was achieved.

For analyzing the crystal orientation of individual grains, Automated Crystallography for TEM software (ACT) provided by EDAX was used. First, the region of interest along the Cu interconnect line was tilted in the TEM over a wide range to identify all the individual grains present in the viewing area (Fig. 3.6). As grain boundaries can go out of contrast under different tilting conditions, this procedure ensured that all the individual grains were identified. The TEM images were saved for reference for subsequent DP acquisition.

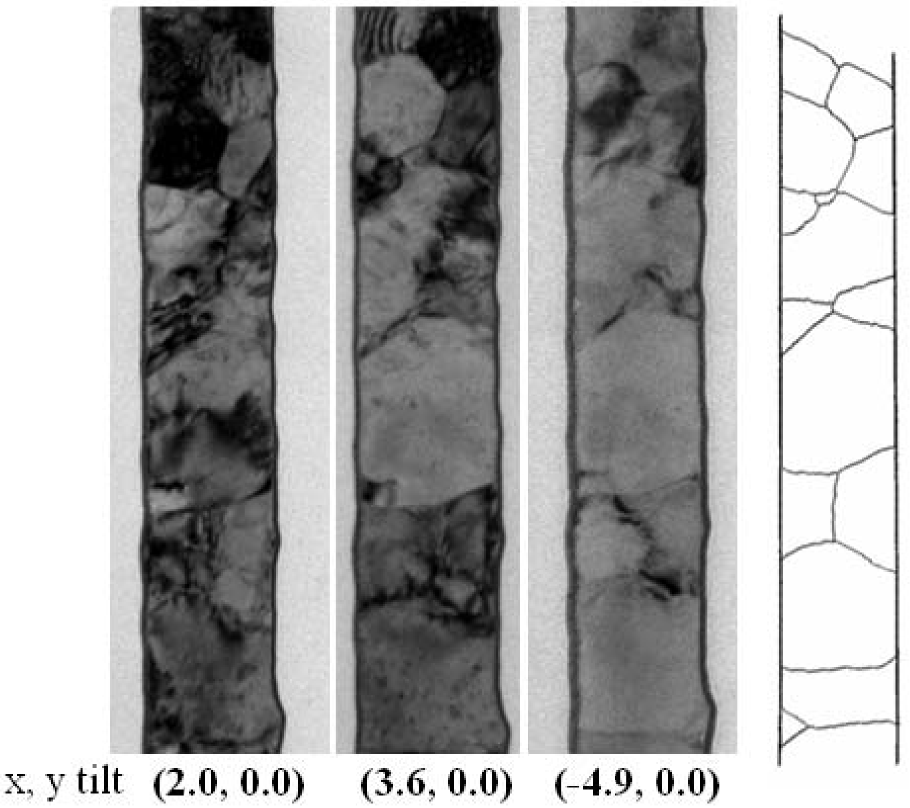


Fig. 3. 6: Sample tilting during TEM operation to identify grain boundaries for ACT orientation analysis

When placing the TEM electron probe over an individual grain, it can be difficult to determine if the probe is solely over a particular grain, particularly in the case of nano-size grains. To overcome this problem, the composite imaging function in the ACT was used. This function allows the user to overlap the probe with the TEM bright field image (Fig. 3.7a), so that the probe can be accurately positioned over a single grain. This prevents the user from acquiring a DP from multiple grains, which would make indexing very difficult. Once the probe is placed over the grain, the DP is obtained. The DP is then automatically indexed using the appropriate Cu materials file available in the database, and the calibrated camera length. Fine adjustments are made using the simulation function to ensure that accurate crystal orientation information is obtained. The resulting information includes crystal orientation, misorientation angles between adjacent grains, and a pole figure (Fig 3.7b).

In order to distinguish between kinematical and dynamical diffraction spots, and to ensure that the indexing is accurate, off-zone axis patterns are tilted to the closest zone-axis, and indexed. The simulation function is used again to simulate the tilting conditions, allowing the user to match the simulated diffraction pattern with the obtained diffraction pattern. Based on these results, the kinematical (forbidden) diffraction spots are identified, and omitted from the analysis.

No efforts were made to measure the 'fifth angle' necessary to fully characterize the local boundary type, as the intentions of this grain orientation measurements was

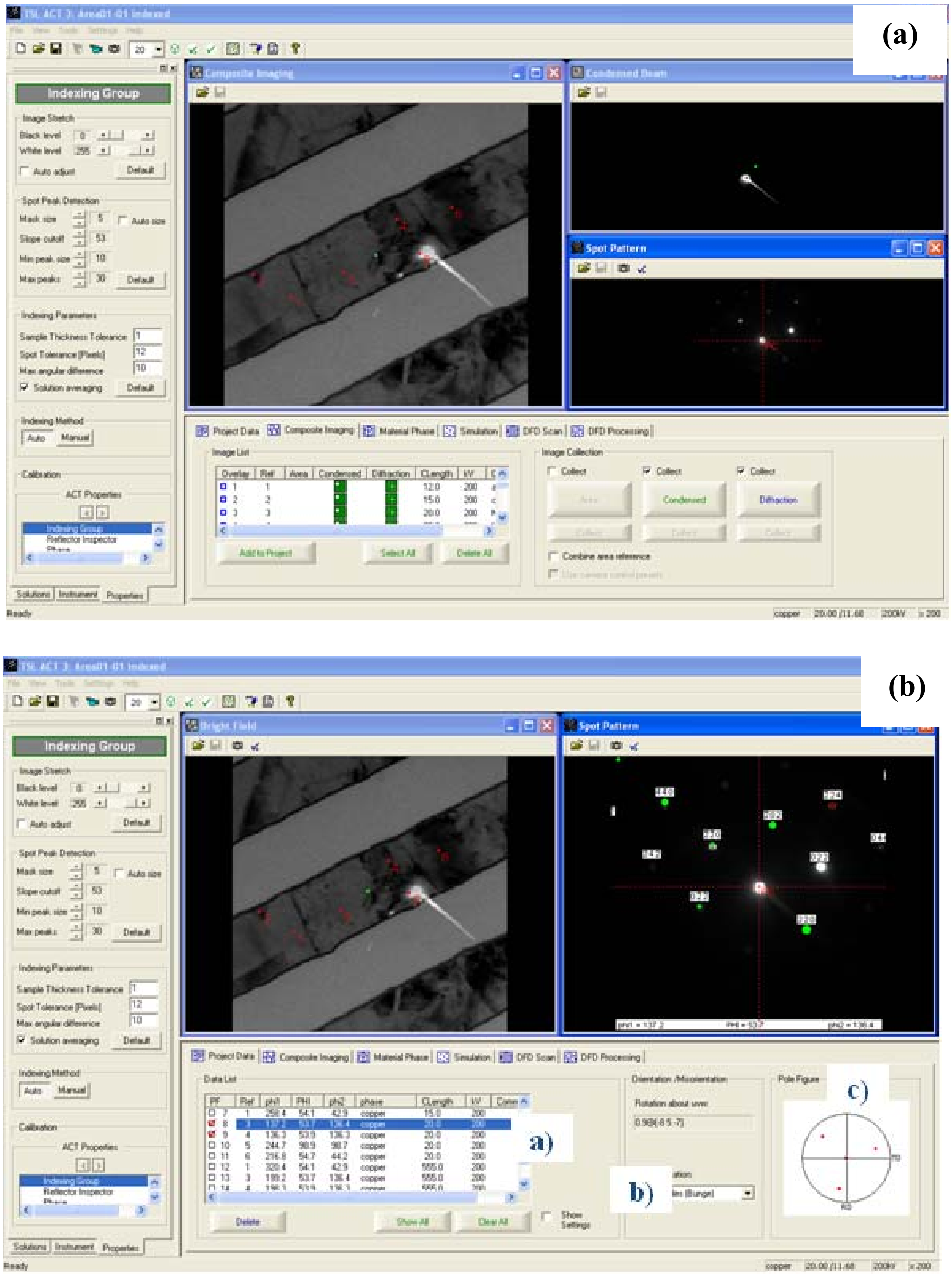


Fig. 3. 7 : (a) The composite function available in the ACT software allows the user to overlap the electron probe over the grain of interest and record the DP (b) DP indexed on ‘Project Data’ window

to conduct FEM simulations of the local stresses. Such local boundary type characterization was not necessary to perform these stress simulations. In addition, it was assumed for simulation purposes that the resulting Cu grains in the TEM sample are columnar in nature.

3.6 CALCULATION OF LOCAL HYDROSTATIC STRESSES BY FEM ANALYSIS

The local hydrostatic stresses present in Cu interconnects due to the misorientation of grains (discussed in Chapter 2) were simulated using OOF2, an FEM software developed by the National Institute of Standard and Technology (NIST). The OOF2 stress simulations were run in a Dell Precision 530 Workstation with a SuSE Linux operating system.

Based on the TEM images, the software "Adobe Photoshop" was first used to identify and illustrate the copper grains along the Cu interconnect lines (Fig. 3.8), Each grain was first designated an arbitrary color. Every pixel in each individual grain must be of a uniform color, as the OOF2 program recognizes each pixel group as an independent object (in this case, as an independent grain). Subsequently, the crystal orientation of each grain, obtained as described in 3.3, and the mechanical properties of copper and TEOS (Table 3.2 and 3.3) were used as input data in the OOF2 program and assigned to each individual grain.

In simulating the hydrostatic stresses, the following assumptions were used:

1. A biaxial stress model (i.e. $\sigma_z = 0$) was considered. Despite the fact that the Cu interconnect lines were subjected to 3D quasi-hydrostatic stresses $(\sigma_x \rangle \sigma_y \rangle \sigma_z)$, σ_x and σ_y are nevertheless the major normal stresses

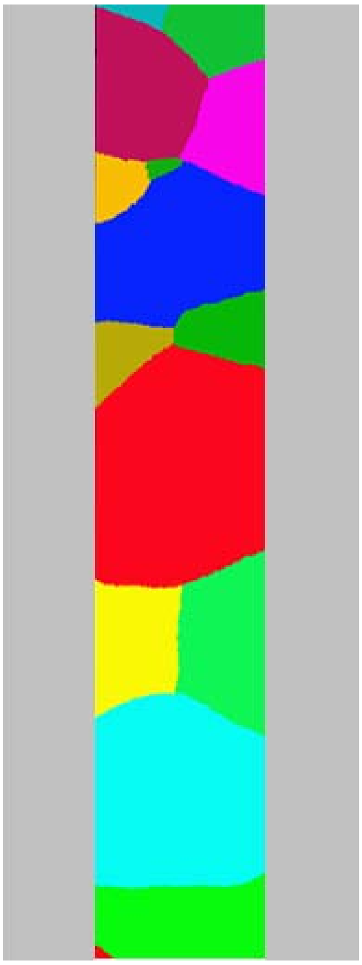


Fig. 3. 8: Each grain in Figure 3.5 is colored for OOF2 analysis. Colors do not indicate particular orientation.

Table 3. 2 : Stiffness Coefficient for Cu [82].

	Stiffness Coefficient of Cu (N/m^2)
C_{11}	16.8×10^{10}
C_{12}	12.1×10^{10}
C_{44}	7.5×10^{10}

Table 3. 3 : Mechanical properties of SiO_2 [83].

Material	Young's modulus	Poisson's ratio
SiO_2	72 GPa	0.2

and thus used in the simulations.

2. The diffusion barrier was removed from the calculations, as the DB is very thin (10~20 nm) and plays a minimal role in affecting the local stresses.

3. The Young's modulus of SiO_2 was used for F-TEOS.

For the FEM analysis, quad meshes were used for the microstructure. A relatively coarse mesh was first constructed, and then refined by creating finer meshes where needed, especially where fine grains were present. Displacements of the Cu interconnect lines due to normal stresses present were used as boundary conditions for the stress simulations. The normal stresses used were previously reported for Cu interconnect lines with similar dimensions [37]. The resulting hydrostatic stresses will be represented using a thermal spectrum, and the same hydrostatic stress legend will be used throughout the dissertation. Since the main interest lies in analyzing the effects of local hydrostatic stresses on Cu interconnects, and most of the discussion will be based on the hydrostatic stress analysis, the term 'stress' used in subsequent chapters will be that of the hydrostatic stress, unless otherwise noted.

3.7 *IN-SITU* THERMAL CYCLING IN HAADF STEM MODE

In order to monitor possible vacancy diffusion paths during void growth, a FEI STEM/TEM equipped with a Gatan heating stage and a High Angle Annular Dark Field (HAADF) detector was used. In the STEM (Scanning Transmission Electron Microscope) mode, a fine electron probe is focused on the sample and scanned over a thin specimen. The inelastic high-angle diffracted electron signal can be measured by the HAADF detector, which is centered on the optic axis and placed below the specimen (Fig 3.9). In this fashion, an image can be obtained, for which the contrast depends on the atomic number (atomic weight) and/or the thickness of the sample [80,84,85]. For a pure material, as in the case of Cu interconnects, the contrast will be only a function of sample thickness.

Thus, in theory, any changes in contrast in the Cu lines, during *in-situ* STEM heating experiments, will provide insight into changes in thickness occurring in Cu, and thereby information on vacancy diffusion paths during void growth. The change in image contrast as a function sample thickness, for a pure material is given by [80];

$$\frac{\Delta I}{I} = 1 - e^{-Q_t \Delta t} = Q_t \Delta t \qquad (3.1\ )$$

where ΔI is the change in intensity over the original intensity I, Q_t the total elastic

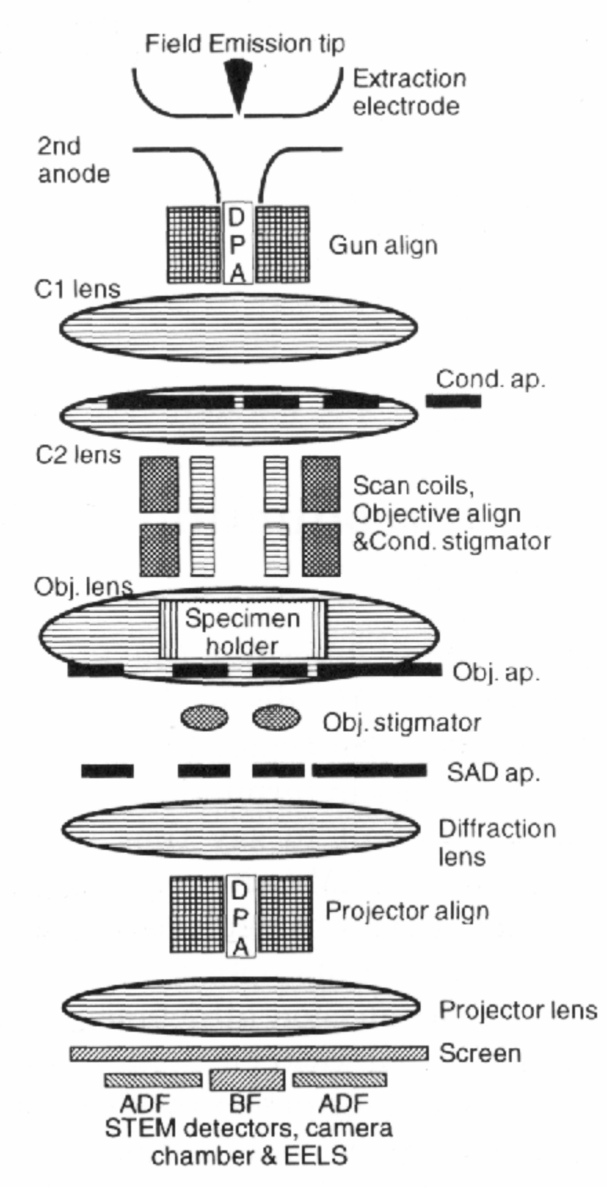


Fig. 3. 9 : Optical configuration in the (S)TEM mode [86].

scattering cross section, and Δt the change in thickness. Q_t can be obtained by;

$$Q_T = N\sigma_T = \frac{N_o \sigma_T \rho}{A} \tag{3.2}$$

where N_o in the Avogadro's number, σ_T the elastic scattering cross section, ρ the atomic density, and A the atomic weight. σ_T can then be obtained by:

$$\sigma(\beta) = \frac{\left[Z\lambda \left(\frac{a_0}{Z^{0.33}} \right) \left(1 + \frac{E}{E_0} \right) \right]^2}{\pi (a_0)^2 \left(1 + \left(\frac{\beta}{\theta_0} \right)^2 \right)} \tag{3.3}$$

where Z is the atomic number, λ the mean-free path for elastic scattering, a_0 the Bohr radius, E_0 the rest mass energy, E the beam energy, β the semi-angle of collection and Θ_0 the characteristic scattering angle given by $\theta_0 = \frac{0.117 Z^{1/3}}{E^{1/2}}$.

In order to minimize diffraction contrast in the image, a camera length of 43 mm and a 70 micron C2 aperture were used.

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3.8 X-RAY DIFFRACTION

The overall texture of the 1.8 micron and 180 nm samples were analyzed using a Phillips X-ray Diffractometer. The 2-theta angle was varied from 20^o to 90^o at a scan rate of 1^o/min with step of 0.05 degrees. The 2-theta range was determined based on the first four diffraction peaks present in a Cu sample (Table 3.4). To compare the 1.8 micron and 180 nm Cu interconnect lines, the samples were sectioned and placed in the XRD so that an equal volume ratio of Cu/dielectric was tested.

Table 3. 4: Standard Cu powder XRD data based on JCPDS reference (04-0836).

Plane	2-theta	Intensity
111	43.29^{o}	100
200	50.43^{o}	46
220	74.13^{o}	20
311	89.93^{o}	17
222	47.57^{o}	5
400	58.45^{o}	3
133	68.25^{o}	9
420	72.35^{o}	8

CHAPTER 4: EXPERIMENTAL RESULTS

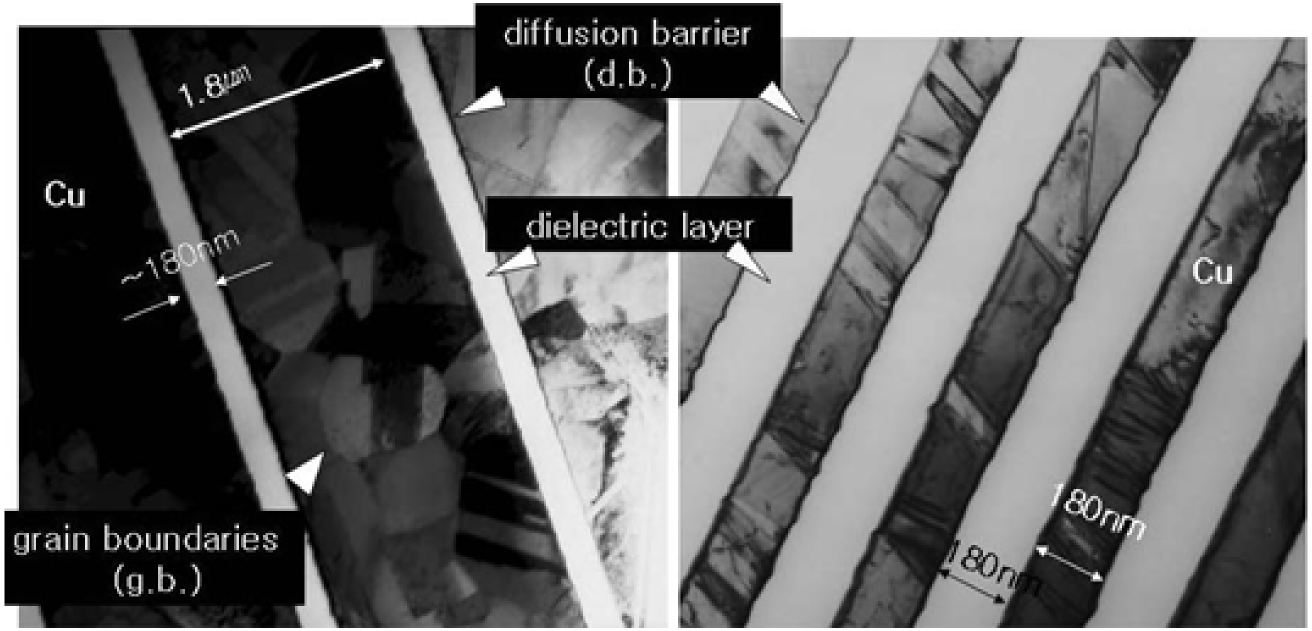
4.1 MICROSTRUCTURE OF CU INTERCONNECTS

4.1.1 Plan view

TEM planar observations of the 1.8 μm and 180 nm CI lines, prior to *in-situ* heating, showed distinct grain structures. The 1.8 μm lines showed predominantly an equiaxed grain structure (Fig. 4.1a) with an approximate grain size of 1 micron. On the other hand, the 180 nm lines exhibited a near bamboo grain structure (Fig. 4.1b). In some cases, multiple grains were observed across the width of the line (Fig. 4.2a). In addition, dislocations (Fig. 4.2b) and annealing twins (Fig. 4.2c) were observed in the 180 nm lines. These twins most likely formed during grain growth of the electroplated Cu lines upon annealing. Such annealing twins were also observed in the 1.8 micron lines.

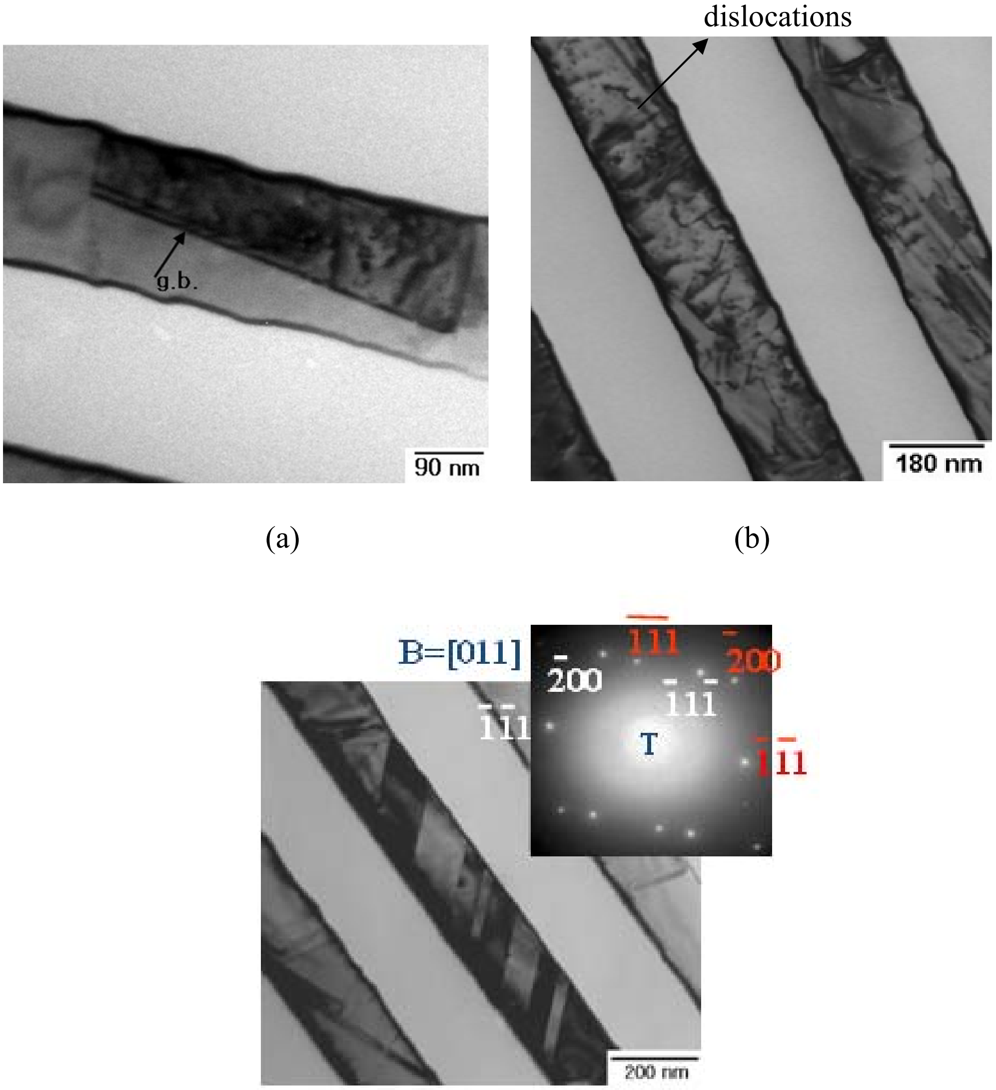
4.1.2 Cross sectional view

Cross section TEM images of the FIB prepared samples (Fig. 4.3a) also showed distinct grain structures for the 1.8 micron and the 180 nm Cu lines. The microstructure of the 1.8 micron Cu interconnects, viewed along the x-direction, revealed the existence of columnar grains extending from the bottom to the top of the trench (Fig. 4.3b).



(a) (b)

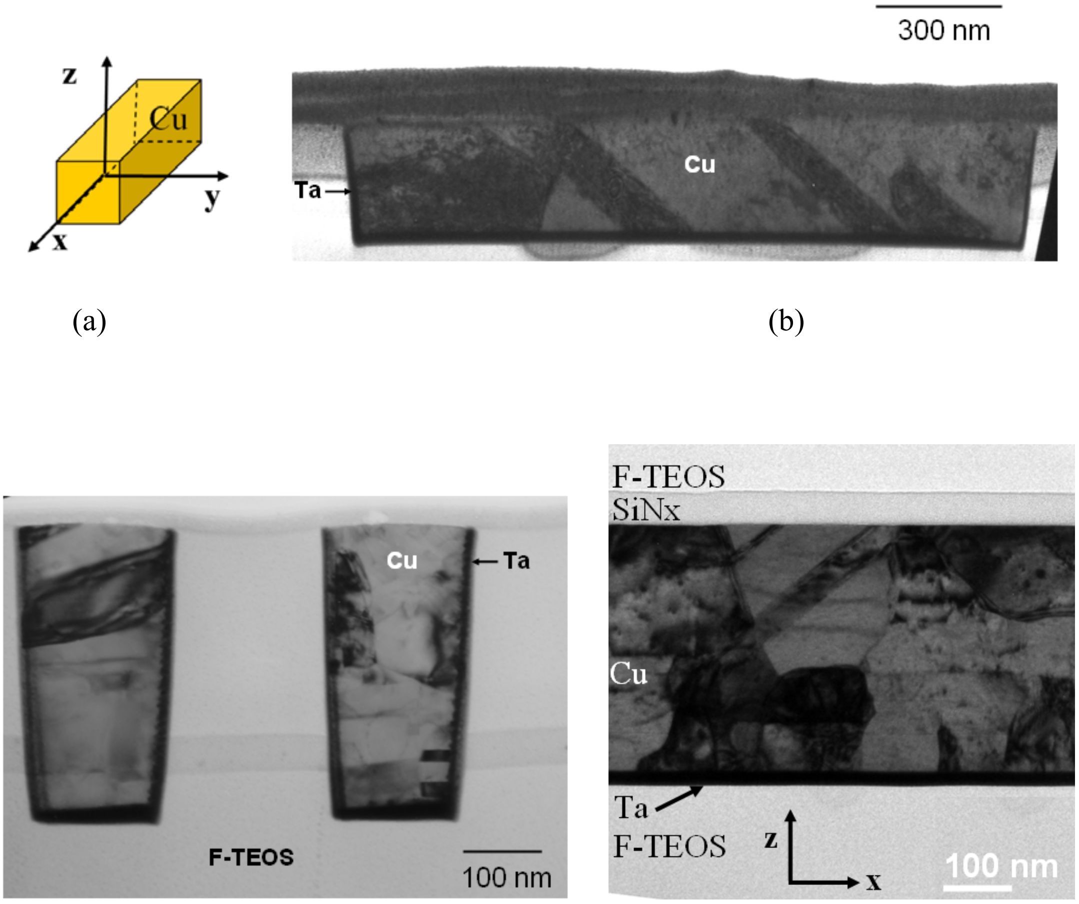
Fig. 4. 1: Plan view TEM image of (a) equiaxed grains in 1.8 micron lines and (b) bamboo grain structure in 180 nm line.



(a) (b)

(c)

Fig. 4. 2: (a) Grains in 180 nm lines that were not completely a bamboo structure (b) pre-existing dislocations (c) annealing twins in 180 nm Cu lines. DP indices in white are the parent reflections, while DP indices darker in color are from the twins



(a) (b)

(c) (d)

Fig. 4.3: (a) Coordinate system used for TEM observation of Cu interconnects (b) cross section image of 1.8 micron interconnects viewed along the x-direction (c) cross section image of 180 nm interconnects viewed along the x-direction (d) 180 nm interconnects viewed along the y-direction

However in the case of 180 nm lines, both cross section images viewed along the x and y direction (Fig. 4.3b-c) showed that multiple grains existed along the thickness (z-direction) of the trench. This is due to the dominant sidewall texture present in narrow Cu lines [73].

4.2 STRESS CHANGES IN CU INTERCONNECTS DUE TO TEM SAMPLE PREPARATION

In order to simulate the change of stresses due to the TEM sample preparation thinning procedure, the electron transparent area thickness and the thickness profile away from the electron transparent area were measured. The electron transparent area was determined after obtaining the deviation parameter s_i from a two-beam condition CBED diffraction pattern and solving the following expression:

$$\frac{s_i^2}{n_k^2}+\frac{1}{\xi_g^2 n_k^2}=\frac{1}{t^2} \tag{4.1}$$

where s_i is the deviation for the 'i'th fringe, n_k an integer, ξ_g the extinction distance, and t the sample thickness. On the basis of equation (4.1), the thickness at the electron transparent area was found to be approximately 50 nm.

The thickness profile measurements, taken away from the electron transparent area, by a Veeco Profilometer, revealed a nearly linear increase in thickness from the electron transparent area at the specimen's center, to a distance 150 μm from the edge of the sample. According to these measurements, R_g was found to be 150 μm (Fig. 3.5). The substrate thickness h_s was assumed to be 80 μm, based on the approximate thickness of the sample after polishing.

Fig. 4.4 compares the relative change in the average stress between the single-layer model (for a homogeneous Cu film) and the multilayer model, which includes the SiO_2 and SiLK dielectric layers. The thickness of the electron transparent area is assumed to be h_e = 50 nm, while the radius R_e is varied from 5 μm to 20 μm. Apparently, the relative change in stress for the multilayer model is reduced, mainly due to the relatively low stiffness in the thick part of the multilayer film containing the dielectric material. It is noted that, while Cu and SiLK have larger coefficients of thermal expansion (CTEs) than Si, TEOS and SiN_x have smaller CTEs. Consequently, the reference stresses in TEOS and SiN_x have the opposite sign of the stresses in Cu and SiLK. This leads to a different trend for the multilayer model with TEOS compared to the other two curves (Fig. 4.4). Also interestingly, although the stiffness of SiLK is much lower than TEOS, the relative change in stress is comparable to that with TEOS. This is again attributed to the opposite stress sign in TEOS, which partly compensates the stress redistribution in the Cu film. Therefore, the stress state in the multilayer thin films is complicated, depending on the relative stiffness of each layer as well as the coefficients of thermal expansion.

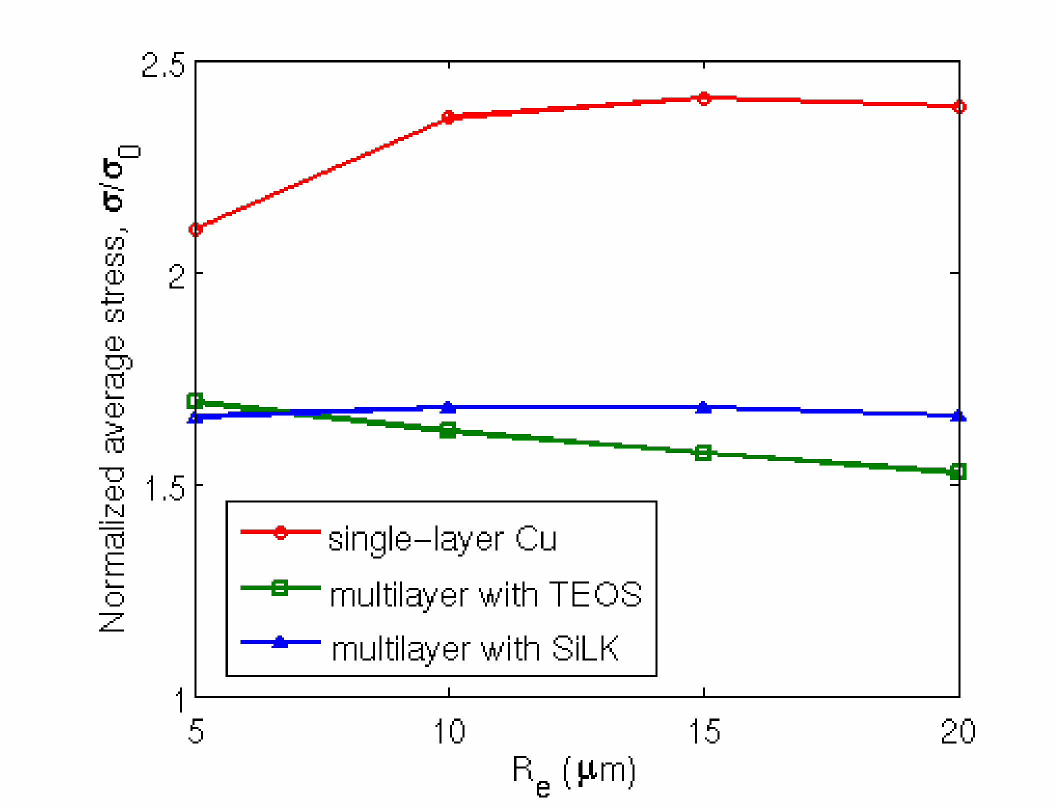


Fig. 4. 4: Comparison of the average radial stresses in multilayer and single-layer models [83].

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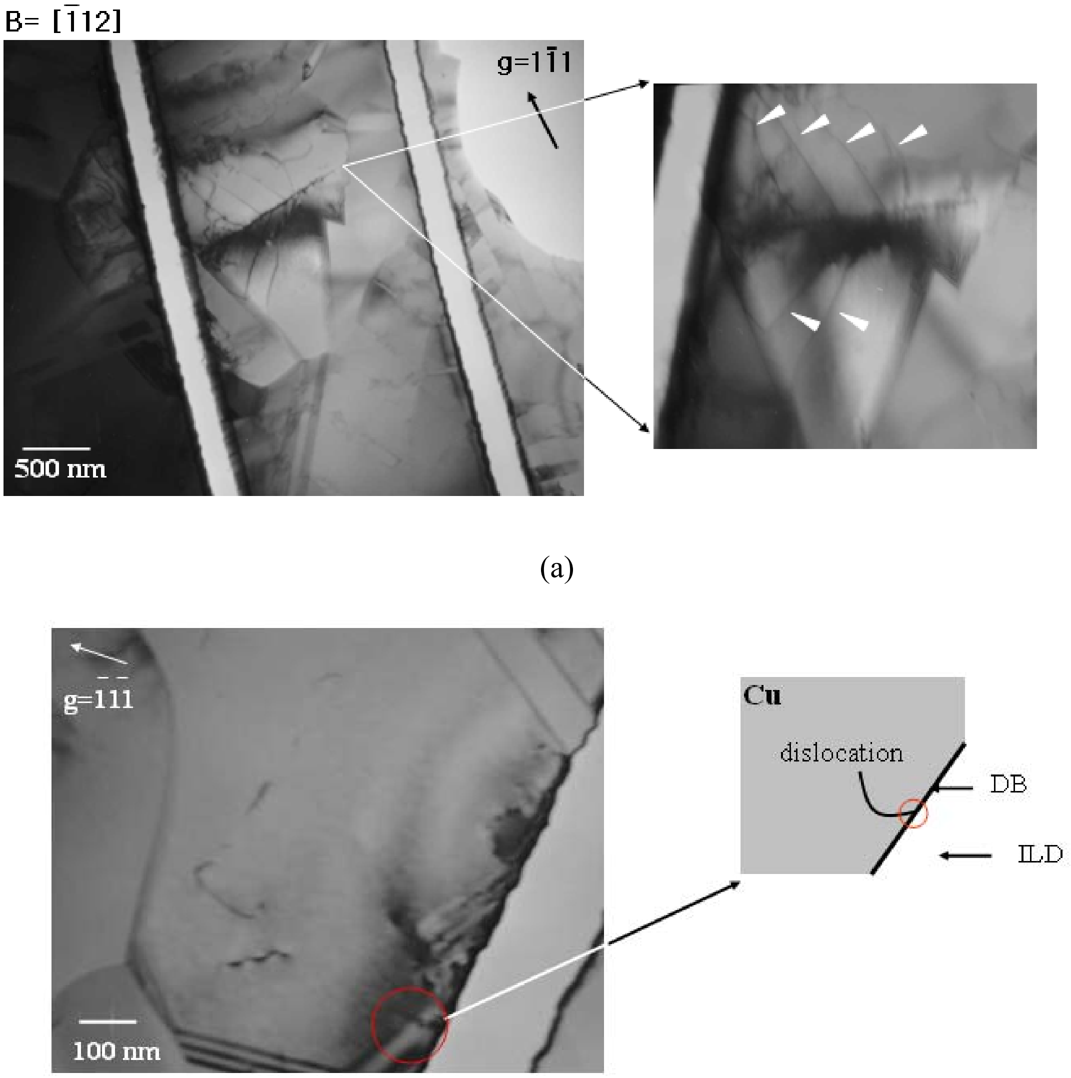
4.3 *IN-SITU TEM HEATING*

4.3.1 Effect of interconnect linewidth on stress relaxation mechanisms under thermal stress

In-situ TEM heating experiments on 1.8 micron lines resulted in the nucleation of dislocations at Cu grain boundaries and consequent motion away from the grain boundaries during the first thermal cycle at around 340^{o}C (Fig. 4.5a). During subsequent thermal cycles, dislocation motion was not observed, most likely due to the fact that stress relaxation has occurred during the 1st cycle. Additional TEM observations showed that existing dislocations at the Cu/DB interface tried to initiate glide (jerky motion), but were pinned due to the good adhesion characteristics between Cu and the Ta DB (Fig. 4.5b).

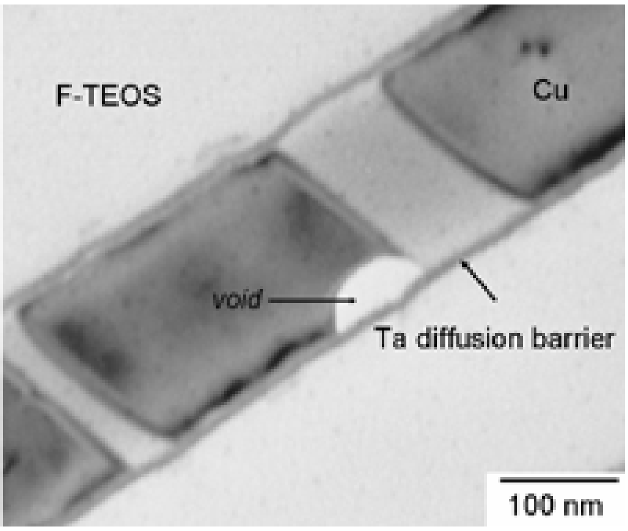
In the case of 180 nm lines, dislocation nucleation and motion was not observed during *in-situ* heating. On the other hand, during the 1st thermal cycle, voids formed at triple junctions where the Ta DB interface meets a Cu grain boundary (Fig. 4.6a-b). Void formation in 180 nm lines always occurred at these triple junctions with the exception of one void (among more than a 100 observed), which formed in the middle of the line at a Cu grain boundary (Fig. 4.7).



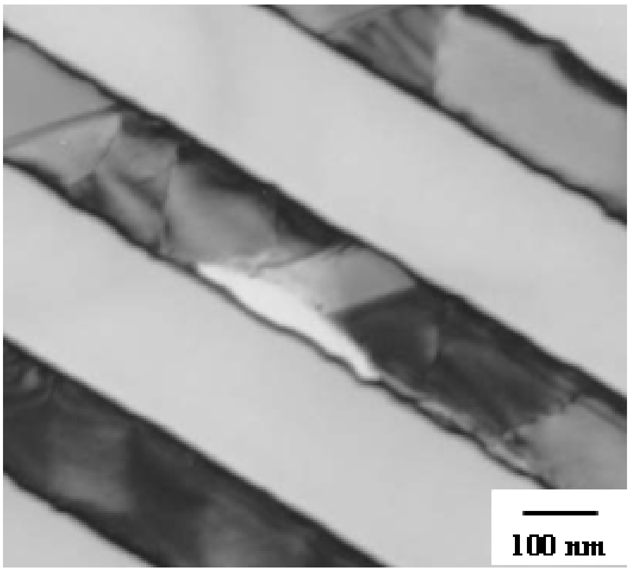
(a)

(b)

Fig. 4. 5: *in-situ* TEM heating results from 1.8 micron interconnects (a) White arrows indicate dislocations nucleating at grain boundaries in 1.8 micron lines during the 1st thermal cycle. (b) Dislocation pinned at the Cu/DB interface during the 1st thermal cycle.



(a)



(b)

Fig. 4. 6: Voids forming at triple junctions where the Ta DB meets a Cu grain boundary.

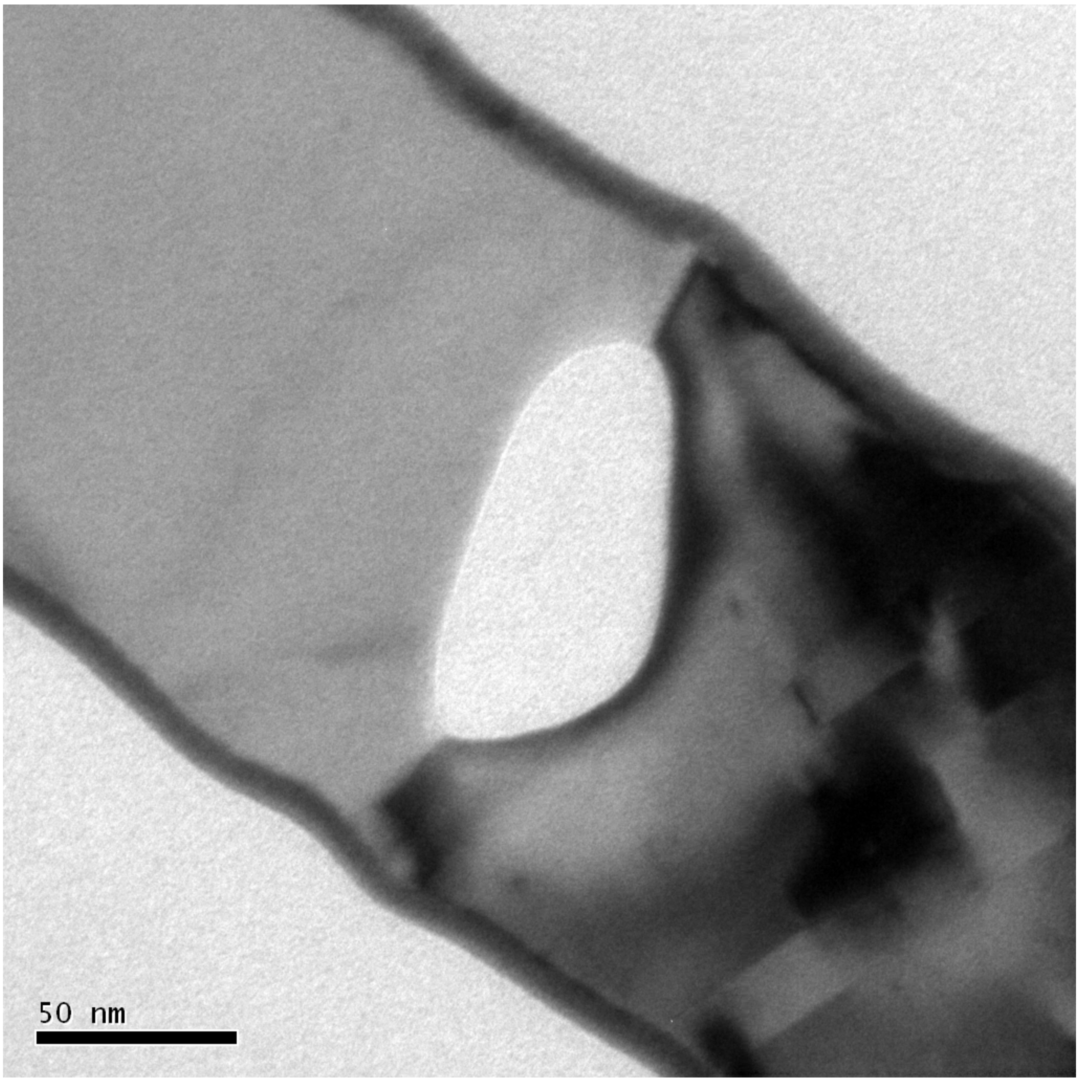


Fig. 4. 7: Void formed in the middle of the line at the Cu grain boundary. This case was the only exception among more than 100 voids observed, where the void nucleated away from the triple junction.

From these *in-situ* heating TEM observations, it is clear that 1.8 micron lines relax stress through dislocation nucleation (plastic deformation), while 180 nm lines relax the stress through void formation.

4.3.2 Void growth in 180 nm Cu interconnects

Upon void nucleation, voids were observed to grow *in-situ* in the TEM under the influence of thermal stress. In some cases, voids propagated completely across the width to a point of complete failure (Fig. 4.8). Figure 4.9 shows a sequence of images captured by *in-situ* TEM, where the void growth characteristics were observed. Fig. 4.9a shows the void immediately after nucleation. Like all voids observed, the void shown in Fig. 4.9a nucleated at a triple junction where the Ta DB meets a Cu grain boundary. As the void propagated, grain A was partially consumed, whereas grain B, seemed to act as a barrier during void growth (Fig. 4.9b). This behavior becomes more evident after some time has elapsed (Fig. 4.9c). In addition, the void assumed an angle of 140^{o} along most of the void length (Fig. 4.9 c-e) until total failure occurred (Fig. 4.9e). Similar TEM observations of different voids during growth revealed consistently the formation of a 140^{o} angle (Fig. 4.10a-b). This characteristic void angle, associated with equilibrium conditions, will be discussed in detail in Chapter 5. In all cases (both 1.8 micron and 180 nm Cu interconnects), no significant Cu oxidation was detected (by DP), and thus it is very unlikely that Cu oxide (if any) affected the *in-situ* TEM heating experiments.

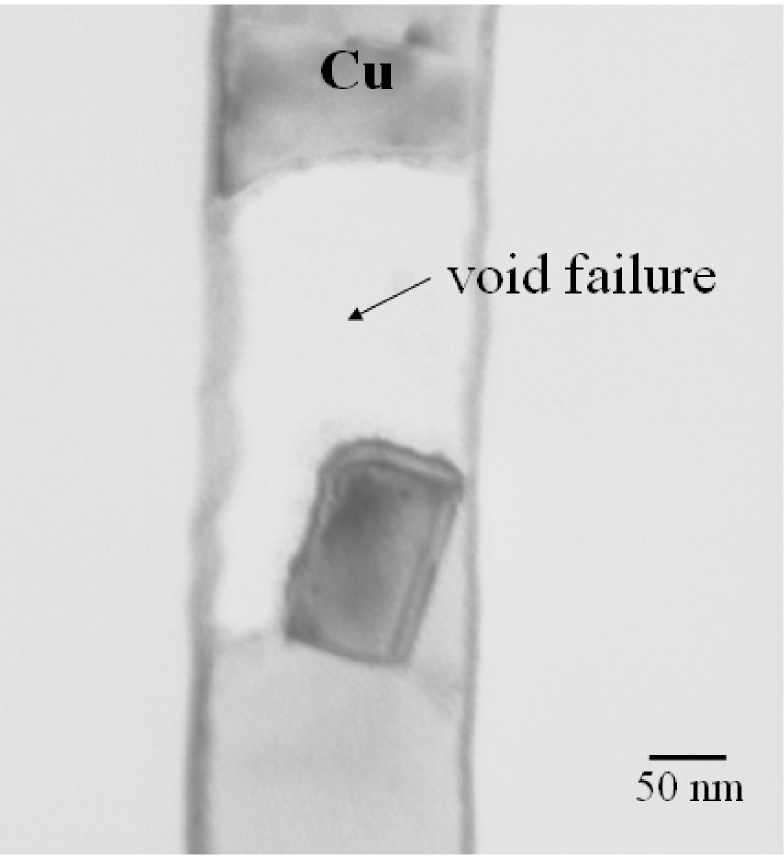


Fig. 4. 8: Void growth to a point of complete failure.

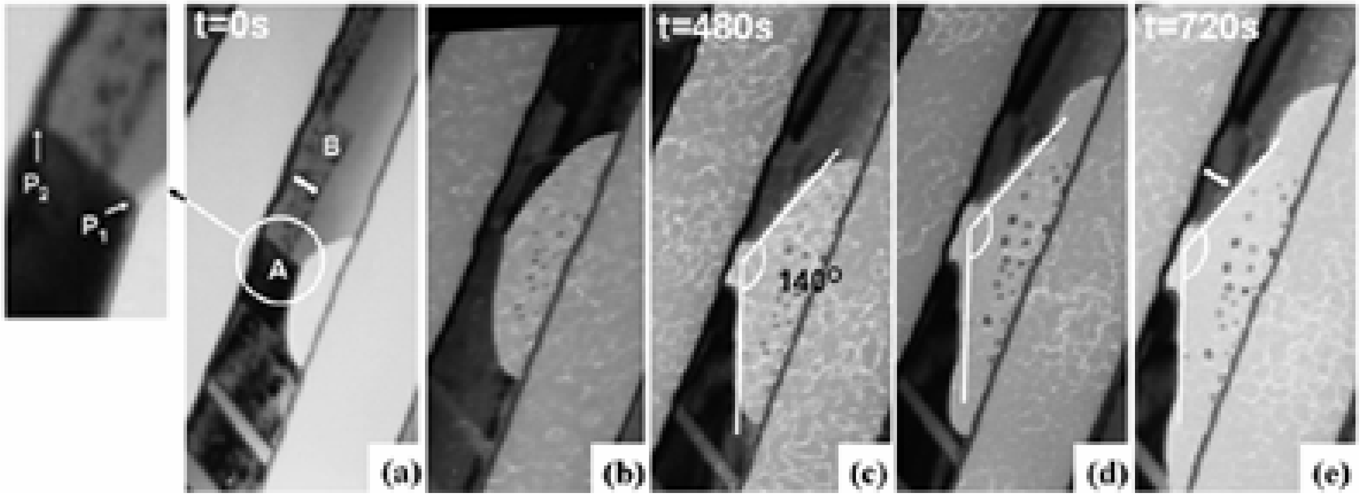
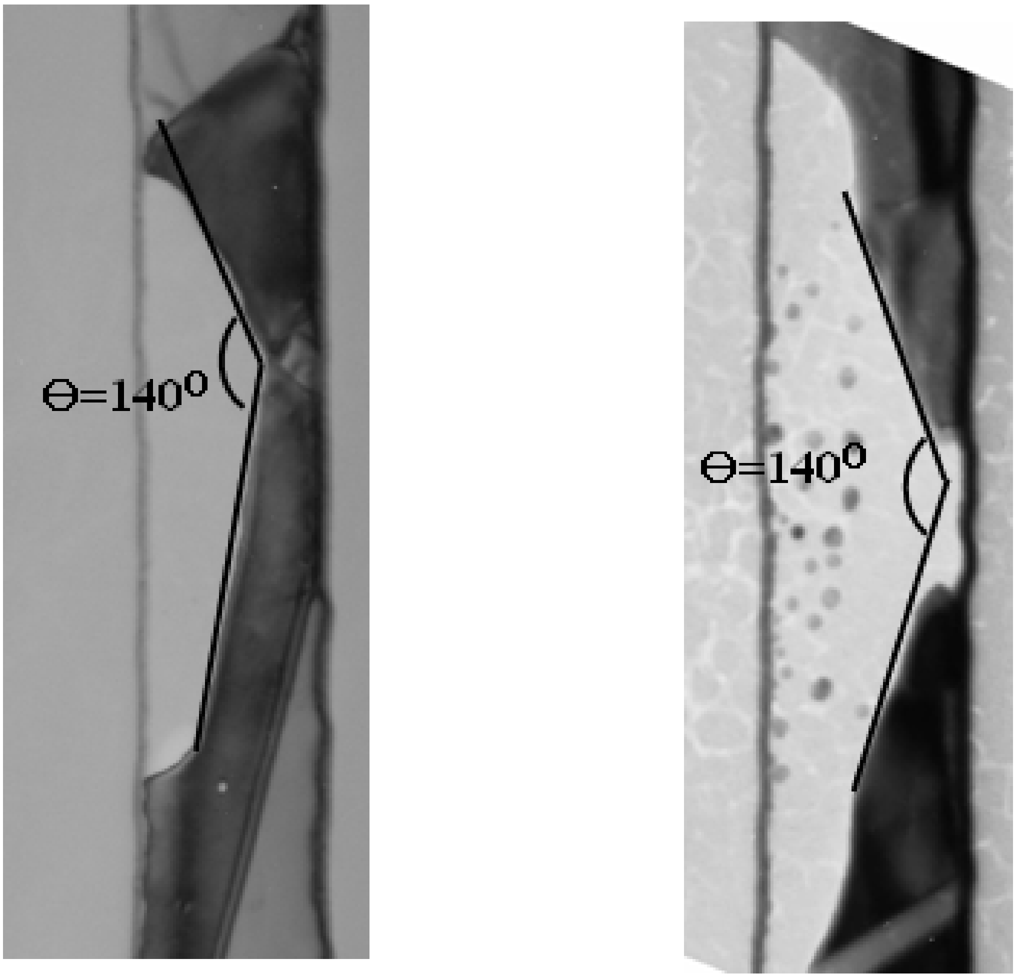


Fig. 4. 9: Void growth during *in-situ* TEM heating (~250^{o}C) recorded over 12 minutes.



(a) (b)

Fig. 4. 10: Void angle formed in two different voids. Void (b) is the void shown in Fig. 4.9.

4.4 GRAIN ORIENTATION IN 180 NM CU INTERCONNECTS

In order to determine the overall texture of Cu interconnect lines, XRD analysis of both the 1.8 micron and 180 nm Cu interconnect lines was conducted (Fig. 4.11). XRD peaks for the {111} and {200} were observed for both Cu interconnect linewidths. When compared with the {111}/{200} intensity ratio (I_{111}/I_{200} = 2.2) obtained for random Cu, both the 1.8 micron and 180 nm Cu interconnect lines exhibit a strong {111} texture (I_{111}/I_{200} = 51.2 for 180 nm lines and I_{111}/I_{200} = 9.09 for 1.8 micron lines), as shown in Fig. 4.11. In the case of the 180 nm lines, a small {220} peak can also be observed.

Despite the strong texture determined by XRD, the local crystal orientation information obtained from ACT provides a different perspective, in particular a distinct texture between the top and the bottom of the lines. The grain orientation associated with the top layer is shown by the inverse pole figure depicted in Fig. 4.12. The results based on 85 grains from 9 different lines, covering an area of approximately 9 microns x 180 nm of area show that although some {111} grains do exist, a significantly more random grain structure is present than the previous XRD results suggest, including {220} and {115} annealing twins. These results are important because the top Cu grain layer and the SiN_x passivation layer interface seem to play a crucial role in void formation.

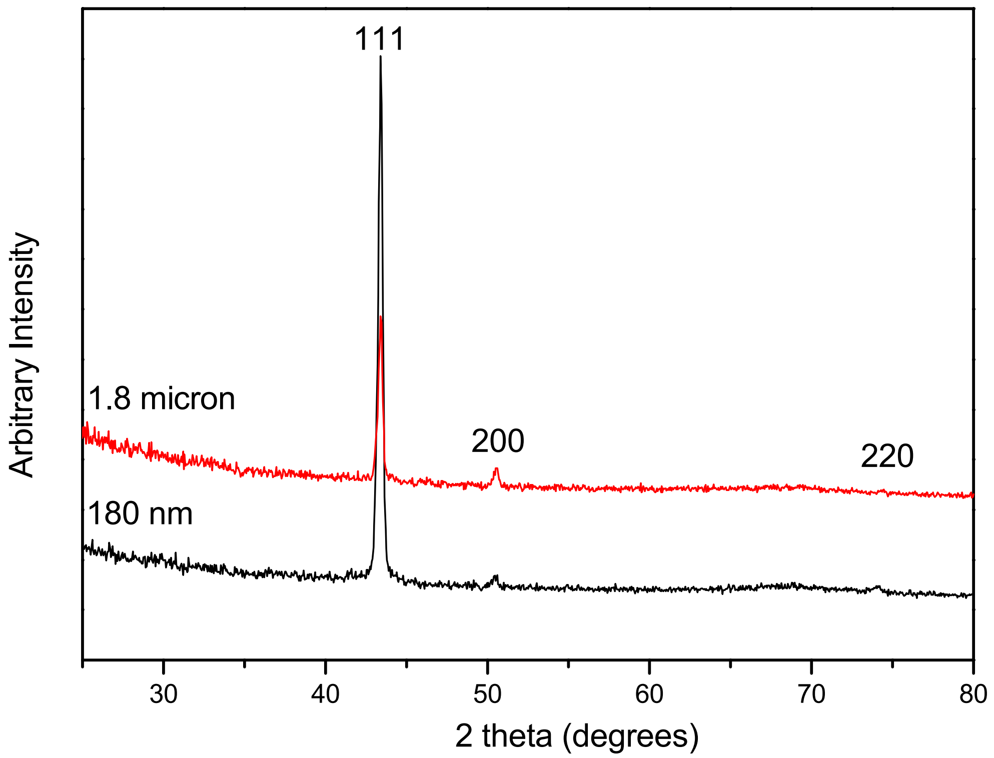


Fig. 4. 11: XRD spectra of 1.8 micron and 180 nm Cu lines.

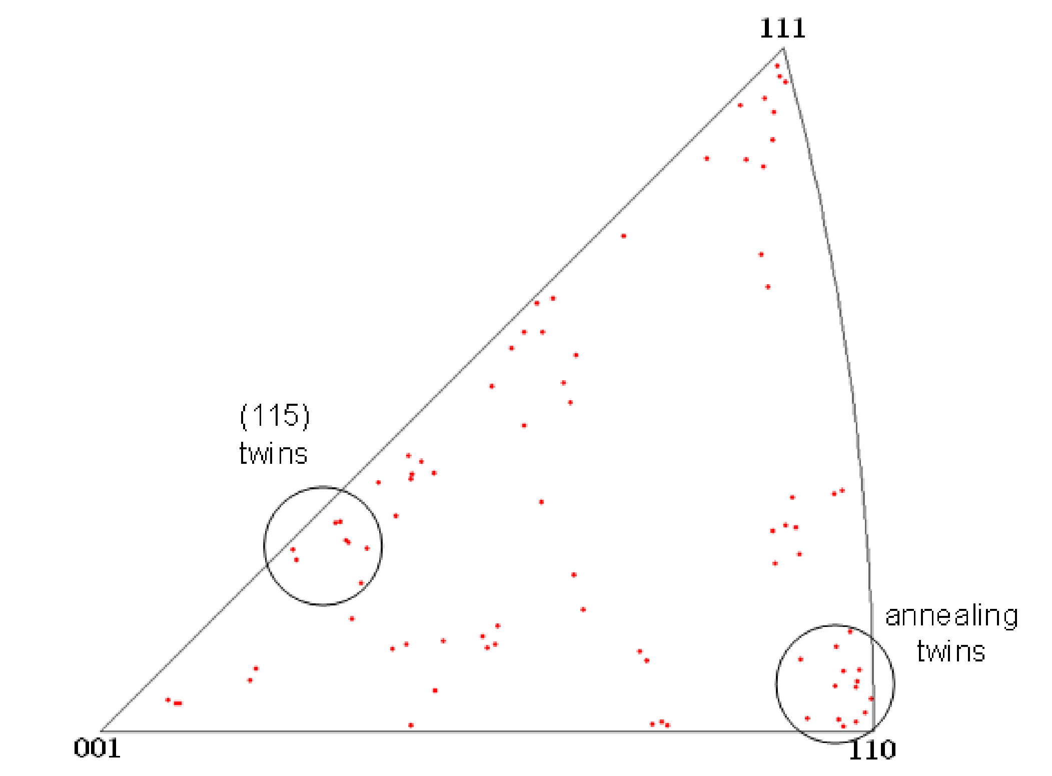


Fig. 4. 12: Inverse pole figure based on 85 grains measured at the top layer of 180nm Cu lines

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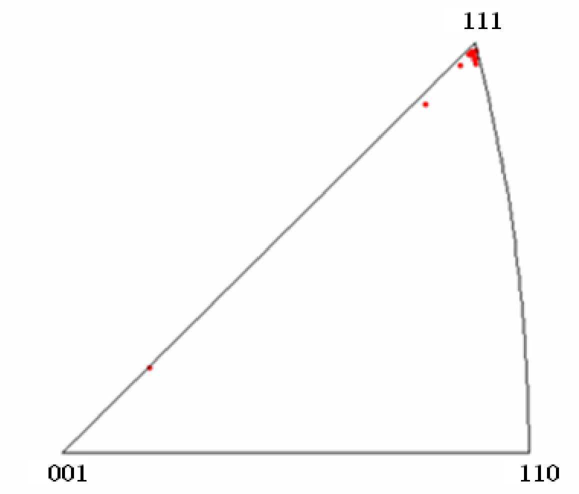
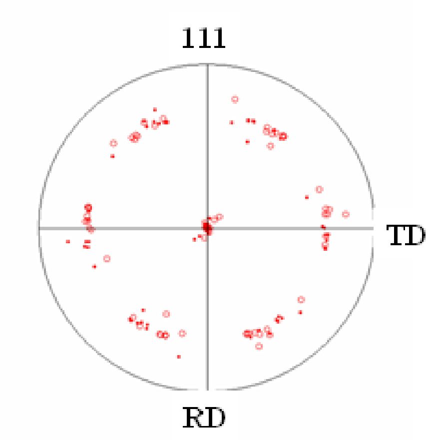
On the other hand, when the top of the 180 nm line was milled for longer times to reveal the bottom section, ACT results show that a strong {111} texture exists (Fig. 4.13a). Indeed, for the 15 grains indexed, with the exception of a single grain oriented along the {115}, all grains exhibited a {111} orientation. Due to the importance of the top layer for void formation, the crystal orientation of the bottom layer was not studied further. A closer look at the {111} grains, both at the top and bottom layers, show that all grains exhibit nearly an identical orientation of the type {111}<220>//RD (Fig. 4.13b).

In summary, the crystal orientation of Cu interconnects using ACT shows that the local orientation at the top of the Cu interconnects is significantly different from the {111} texture suggested by XRD. The ACT software also proved to be effective in indexing very small grains only a few tens of nanometers in diameter (Fig. 4.14).

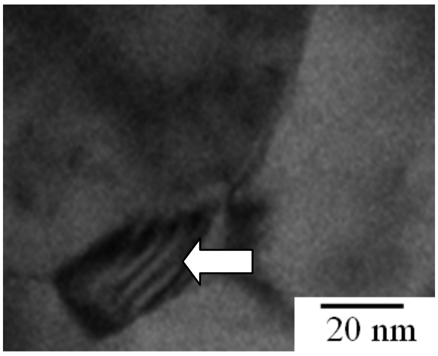


(a)

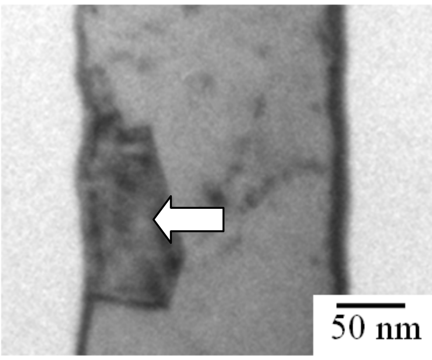


(b)

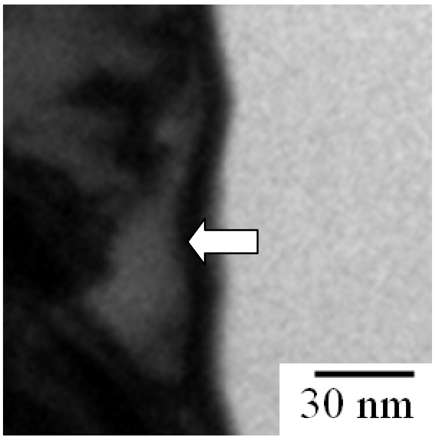
Fig. 4. 12: (a) Pole figure of 15 grains from the bottom layer of the 180 nm Cu interconnect (b) Pole figure of all {111} type grains indexed in this study



{111}<3 2 5>//TD



{7 8 0}<8 7 10>//TD



{13 14 16}<4 2 5>//TD

Fig. 4. 14: Crystal orientation of nanoscale grains indexed using ACT.

4.5 CALCULATION OF LOCAL HYDROSTATIC STRESSES BY FEM ANALYSIS

The local hydrostatic stress along the Cu interconnect lines was simulated according to the experimental procedure used for the OOF2 software outlined in Chapter 3. The crystal orientation obtained from ACT (section 4.4) was used as input data in the OOF2 software, which takes into account the strong anisotropy of Cu, namely a variation in the elastic modulus from 67 GPa along the [001] direction to 190 GPa along the [111] direction (Fig 2.22)

Since the ultimate purpose of the OOF2 stress simulations is to correlate the local stress ('stress' refers to hydrostatic stress unless otherwise noted) along the Cu interconnects lines with void formation, the boundary conditions should be selected for the temperature at which voids were observed to form. As void formation occurred in the range 220-250 ^oC, an average temperature of 230 ^oC was used for the calculations. The normal stresses at this temperature, namely σ_x =262 MPa and σ_y =191 MPa, were obtained from Ho *et. al.* [30] and used as boundary conditions.

Assuming a 2D model and the aforementioned boundary conditions, the stress analysis performed by OOF2 in the 180 nm lines revealed a range of quasi-hydrostatic stresses from 270 MPa to 420 MPa (Fig. 4.15). The stress legend shown in Fig. 4.15(a) will apply to all stress contour maps shown hereinafter in this thesis. In

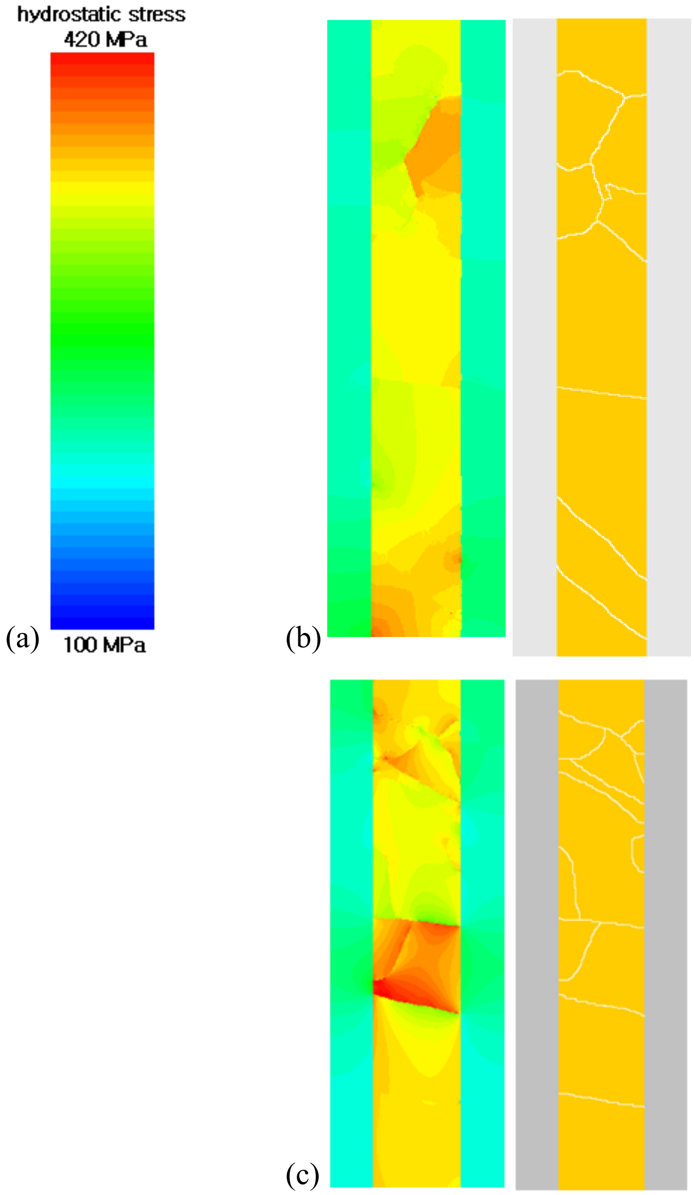


Fig. 4. 15 : (a) Range of stresses calculated. (b)-(c) Stress distribution in 180 nm Cu line at 230^{o}C.

particular, high local hydrostatic stresses are frequently observed at triple junctions, where a Cu grain boundary meets the DB interface. A closer look at the calculated normal stresses show that σ_z is quite significant even in the absence of σ_z in the boundary conditions. In addition, for the regions along the 180 nm lines where a sequence of annealing twins is present, the simulations show that the local stresses fluctuate drastically at the various triple junctions depending on the angle of the twin boundary with respect to the x-y coordinates (Fig. 4.16).

In order to observe the effect of local stresses on void formation, *in-situ* TEM heating experiments were performed on 180 nm lines previously analyzed by ACT to determine the local grain orientation. Subsequently, the local stresses were simulated to correlate the sites where void formation occurred with the calculated stresses. Figures 4.17-4.22 show the results of three different *in-situ* heating TEM experiments.

The results of the first experiment are shown in Fig. 4.17. The various colors were used to identify individual grains, and do not indicate any particular orientation. Of the nine available triple junctions present in the Cu interconnect line, void formation occurred at the triple junction between grains *a* and *b* (Fig. 4.17a). Grain 'a' has an orientation of $\{11\,5\,1\} < \bar{3}\,8\,\bar{7} > // TD$ while grain 'b' has a crystal orientation of $\{0\,2\,3\} < 13\,\overline{12}\,8 > // TD$. The grains are 7.13^{o} and 5.18^{o} away from {012}, respectively. As shown in Fig. 4.17b-c, the junction between grains *a* and *b* area is characterized by a high local stress. In addition, a careful observation of the stress

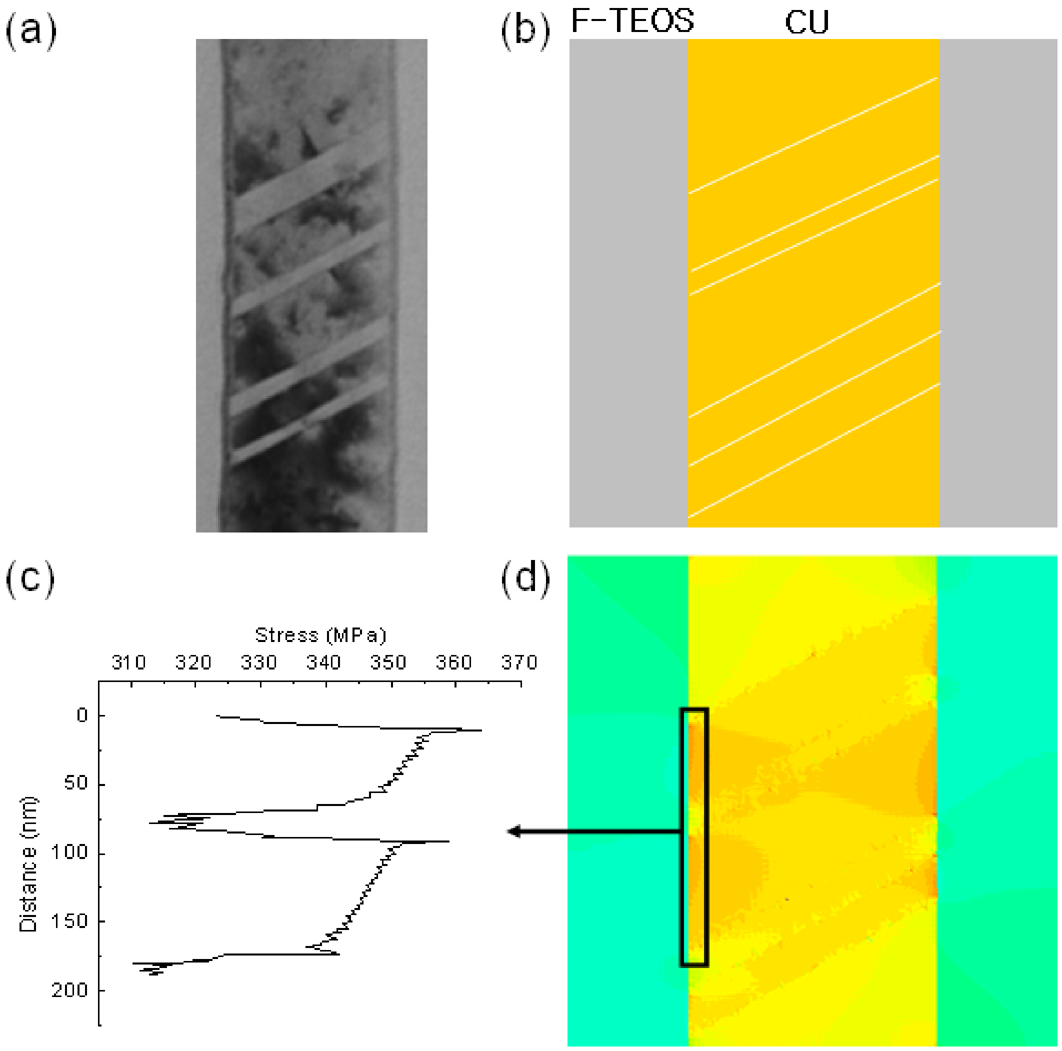
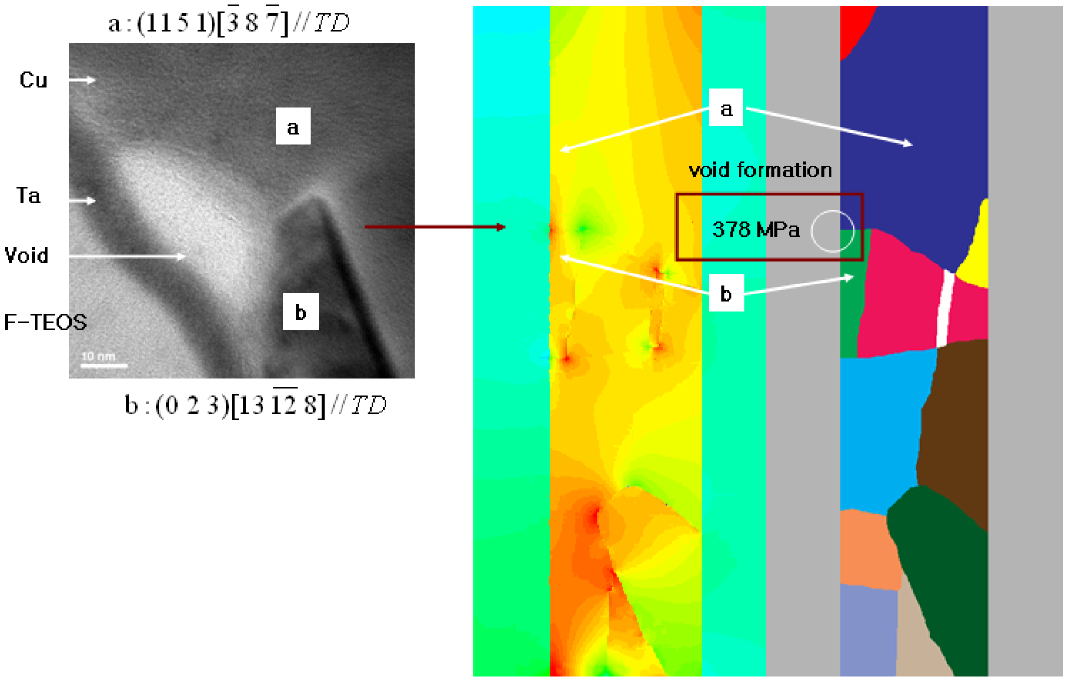


Fig. 4. 16 : (a) TEM image of annealing twins (b) Schematic diagram showing the location of twin boundaries (c) Stress distribution within the region marked by the box (d) Stress distribution map



(a) (b) (c)

Fig. 4. 17: (a) TEM image of void forming between grain a and b (b) Stress contour map of interconnect line (c) Schematic diagram of the 180 nm Cu interconnect. The void formed with the white circle at a triple junction.

distribution in the Cu interconnect line shown in Fig. 4.17, along the left edge of the Cu line, shows that the highest stress exists at the site where void formation occurred (Fig. 4.18). The stress values at the very bottom and top of the Cu interconnect line should be disregarded, as these values are artifacts caused by the truncation of material.

A second experiment is show in Fig. 4.19. In this case, the site where void formation occurred first at the triple junction where grains ‘a’ and b meet. Grain *a* has an orientation of $(\overline{26}\,\overline{24}\,\overline{27})[\bar{3}\,1\,2]//TD$, while grain ‘*b*’ has an orientation $(\bar{6}\,17\,8)[14\,\bar{4}\,19]//TD$. These grains are 2.78^{o} away from $(\bar{1}\,\bar{1}\,\bar{1})$ and 6.50^{o} from $(\bar{1}\,2\,1)$, respectively. Interestingly, the void formation site did not coincide with a point of high local stress according to the 2D simulations (Fig. 4.20).

Finally, the results from the third experiment are shown in Fig. 4.21. Void formation occurred at the triple junction between grains ‘a’ and ‘b’, which show an orientation of $(\bar{5}\,26\,\bar{2})[10\,2\,1]//TD$ and $(15\,4\,\bar{5})[\overline{10}\,\bar{5}\,\overline{34}]//TD$, respectively. These orientations are 11.7^{o} away from {010} and 3.35^{o} away from $(3\,1\,\bar{1})$ respectively. In this case, the location where void formation occurred did not exhibit the highest local stress along the edge of the Cu interconnect line, but a very high stress gradient can be observed (Fig. 4.22).

To evaluate the influence of void formation in the distribution of thermal stresses,

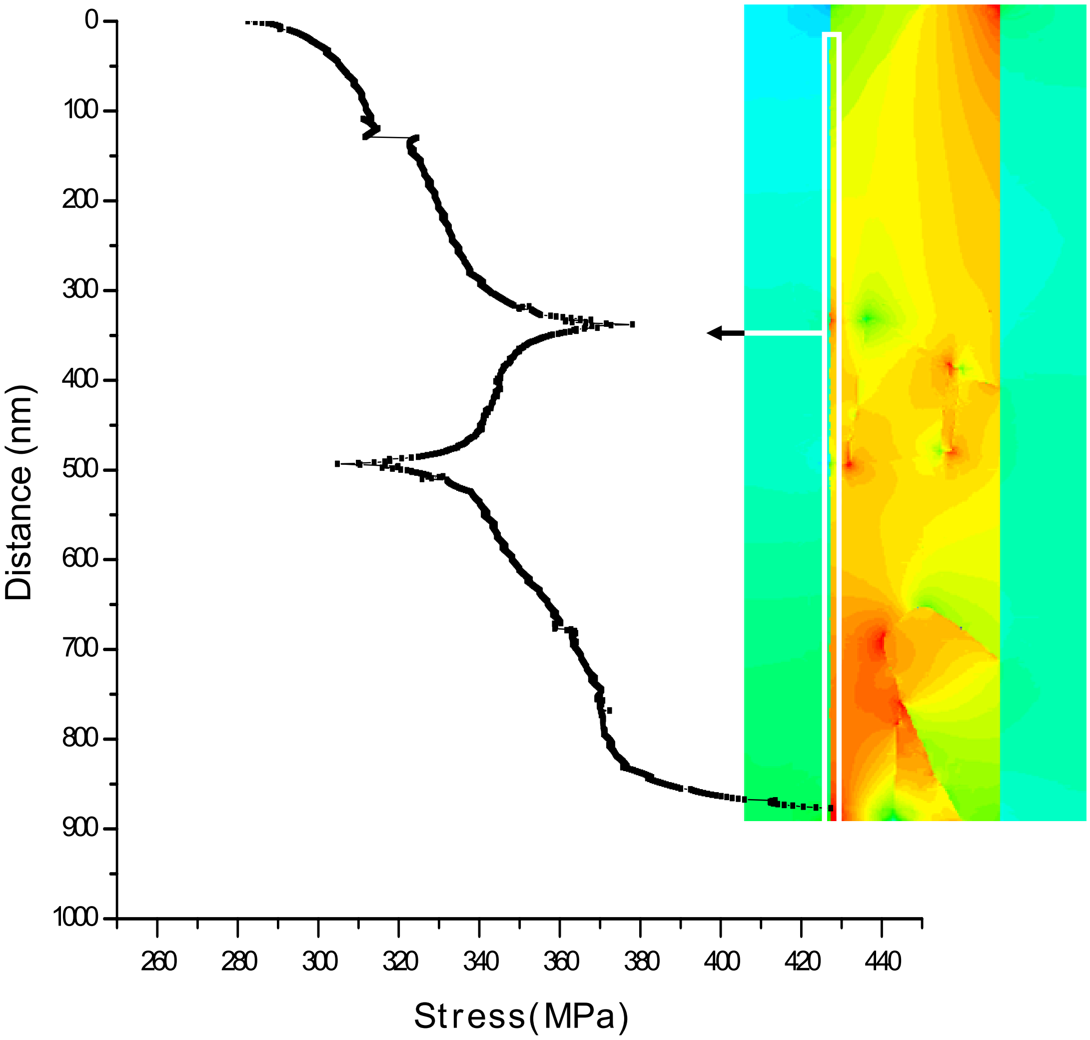
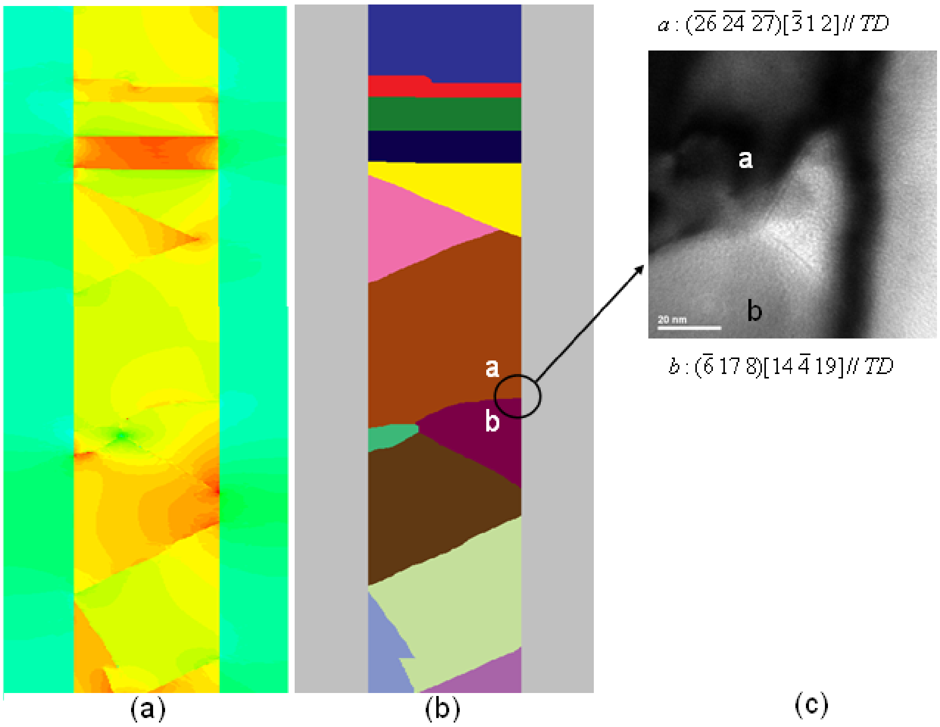


Fig. 4.18: Local stress distribution along the left edge of the 180 nm Cu interconnect shown in Fig. 4.17



(a) (b) (c)

Fig. 4. 19: (a) Stress contour map (b) Schematic diagram of the 180 nm Cu interconnect. (Void formed in the area surrounded by the black circle, at a triple junction) (c) TEM image of void

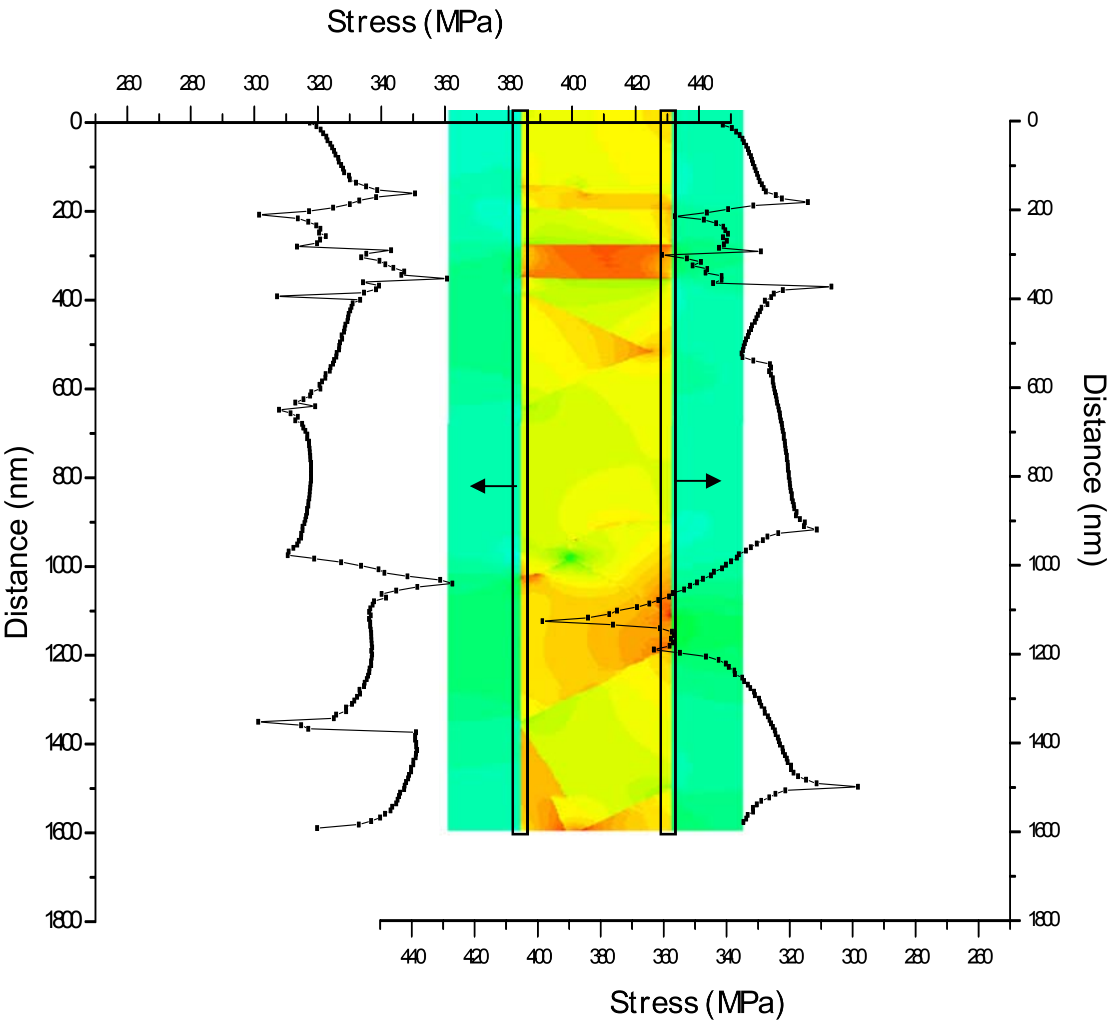


Fig. 4. 20: Stress distribution along the two Cu interconnect edges. Each graph is from the boxed area shown in stress contour map.

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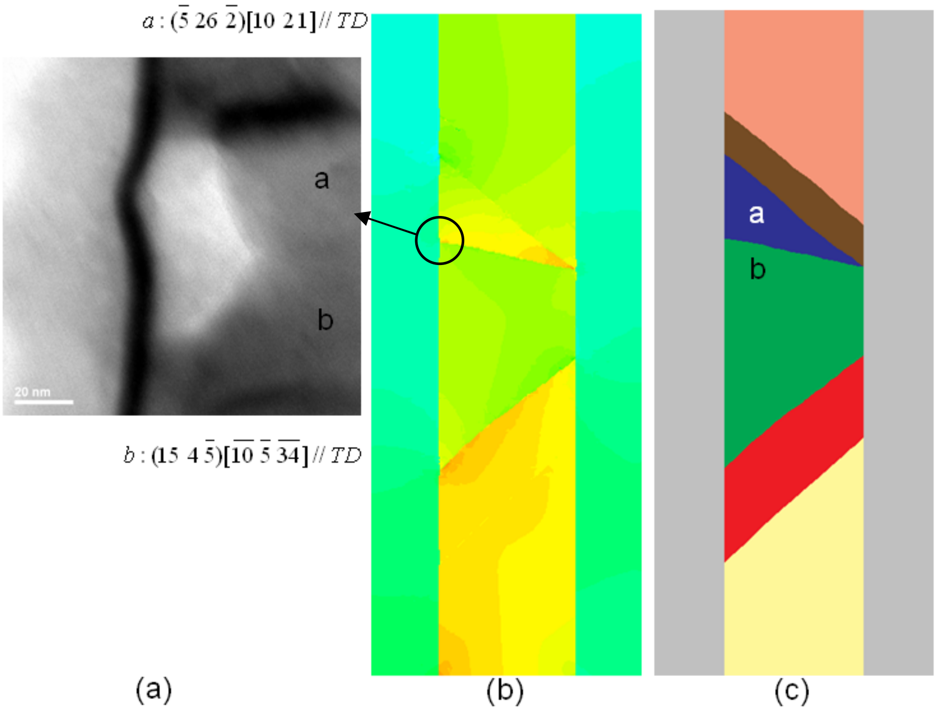

Fig. 4.21: (a) TEM image of void (Void formed within black circle in b) (b) Stress contour map (c) Schematic diagram of the 180 nm Cu line

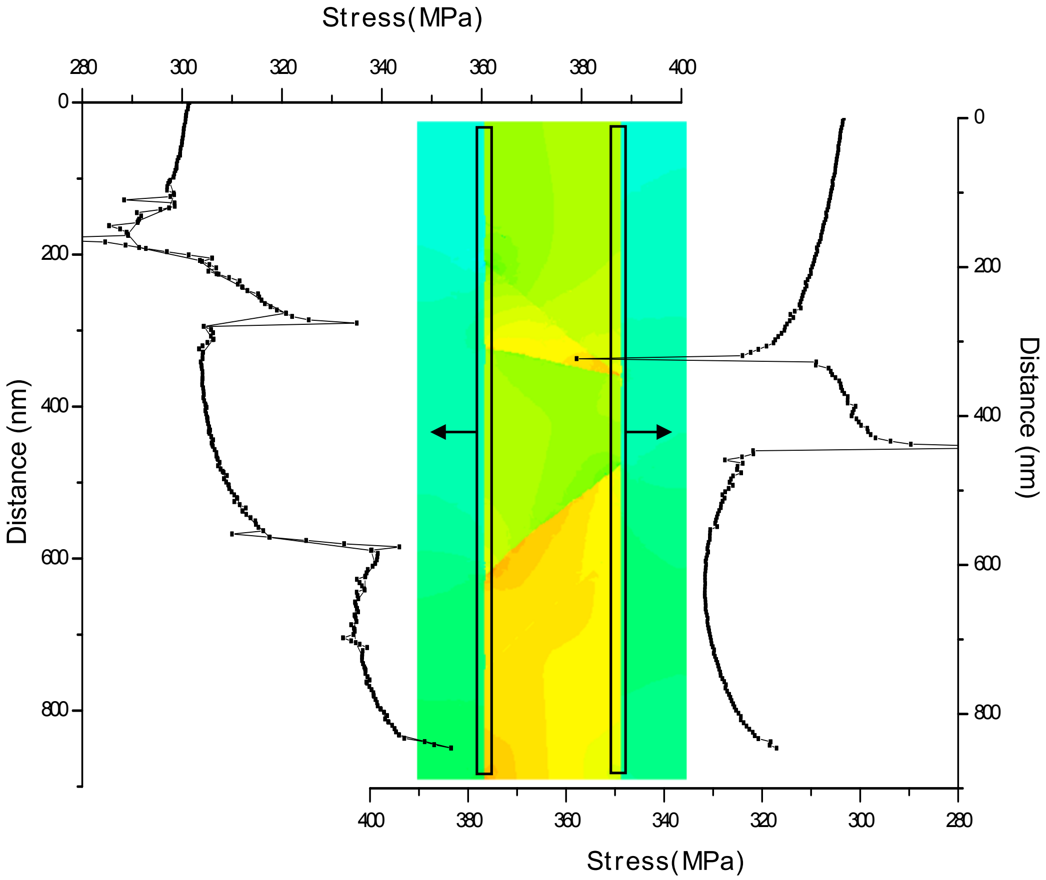

Fig. 4.22: Stress distribution along both edges of Cu line. Each graph is from the boxed area in the stress contour map.

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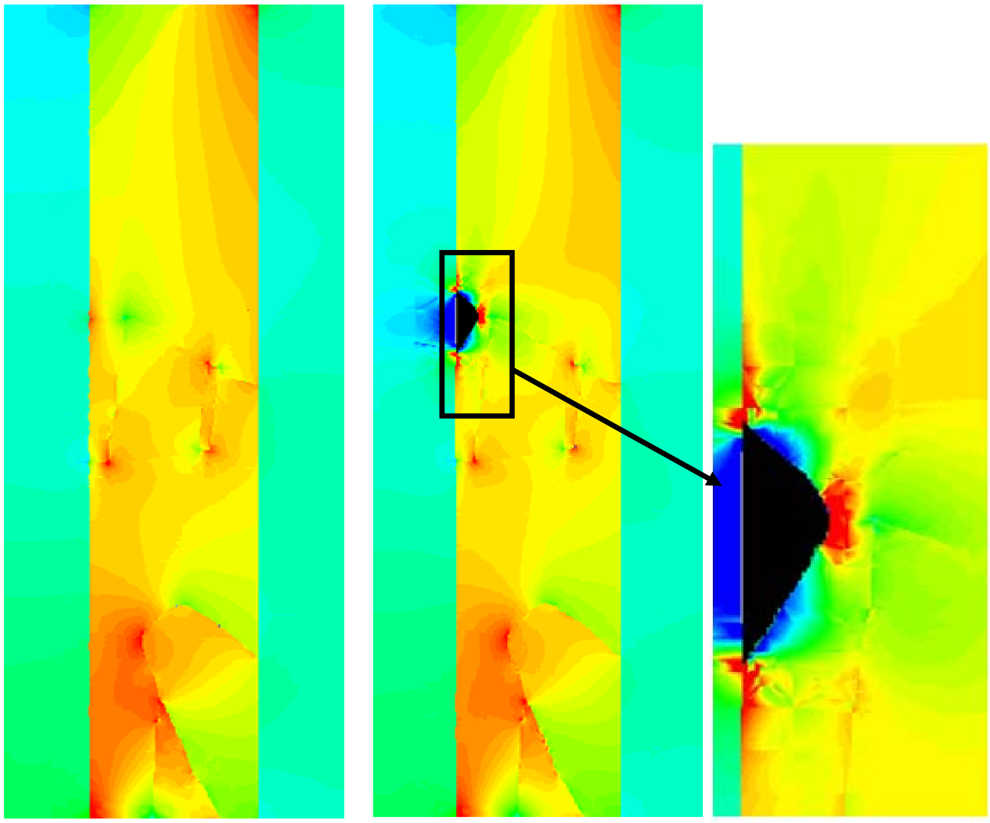
additional simulations were done on the Cu interconnect line shown in Fig. 4.17, after void formation had occurred. This is shown in Fig. 4.23. Overall, the stresses remain the same along the line, except in the region where the void was formed. In this area, high local stresses were observed at each void corner, while lower stresses were observed at the void sides. The local stresses at the corners (500 MPa-700 MPa) were much higher than the maximum stress of 430MPa observed in several Cu lines prior to void formation. Fig. 4.24 and Fig. 4.25 show that the high local stresses drop exponentially away from the void corners.

In addition to the hydrostatic stresses, the deviatoric stresses were also calculated from the simulated normal stresses given by the OOF2 program. The deviatoric stresses can be calculated by subtracting the hydrostatic stress from the normal stress. Based on the 2D stress simulation results obtained in this chapter, the deviatoric stresses were on the order of only a few MPa (5MPa at most). The significance of the low deviatoric stresses will be discussed in Chapter 5.1.



(a) (b) (c)

Fig. 4. 23: Local stress distribution (a) before and (b) after void formation (c) enlarged image of void in b)

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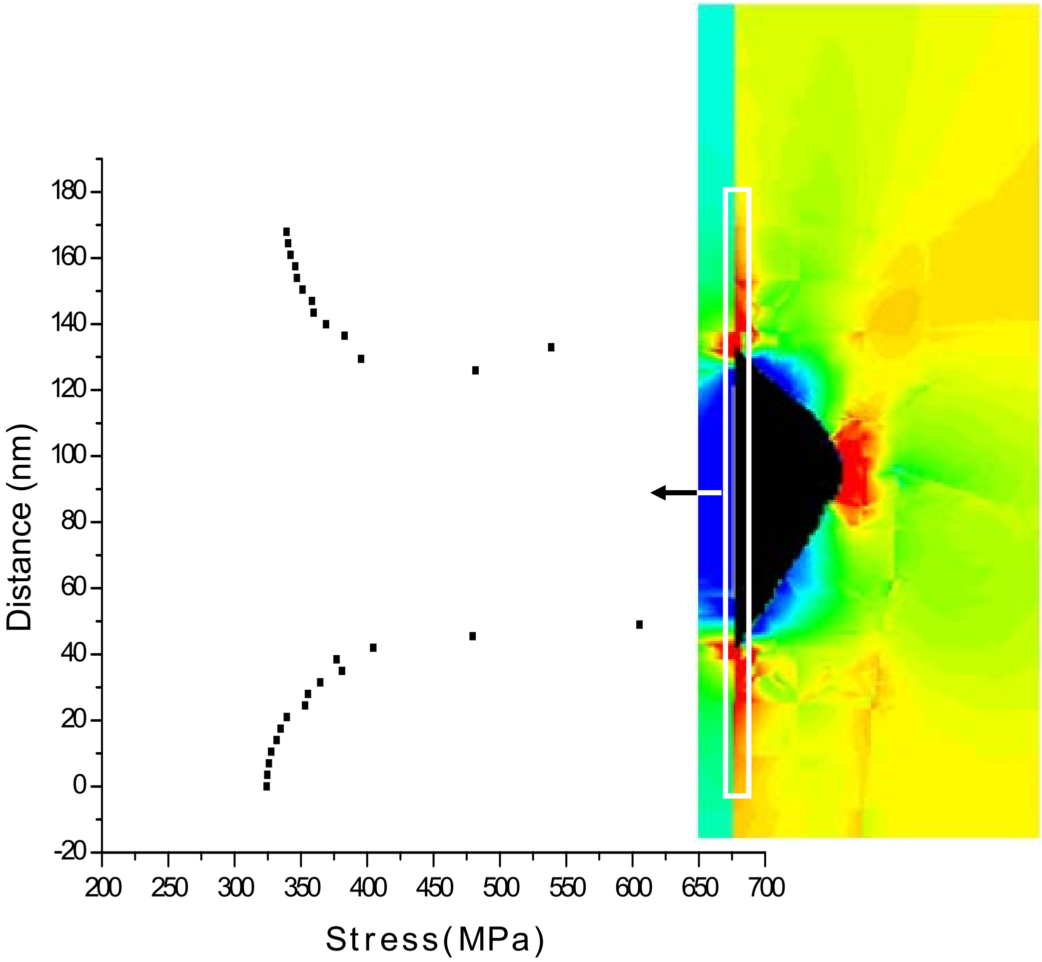

Fig. 4. 243: Local stress distribution along the edge of the Cu interconnect after void formation.

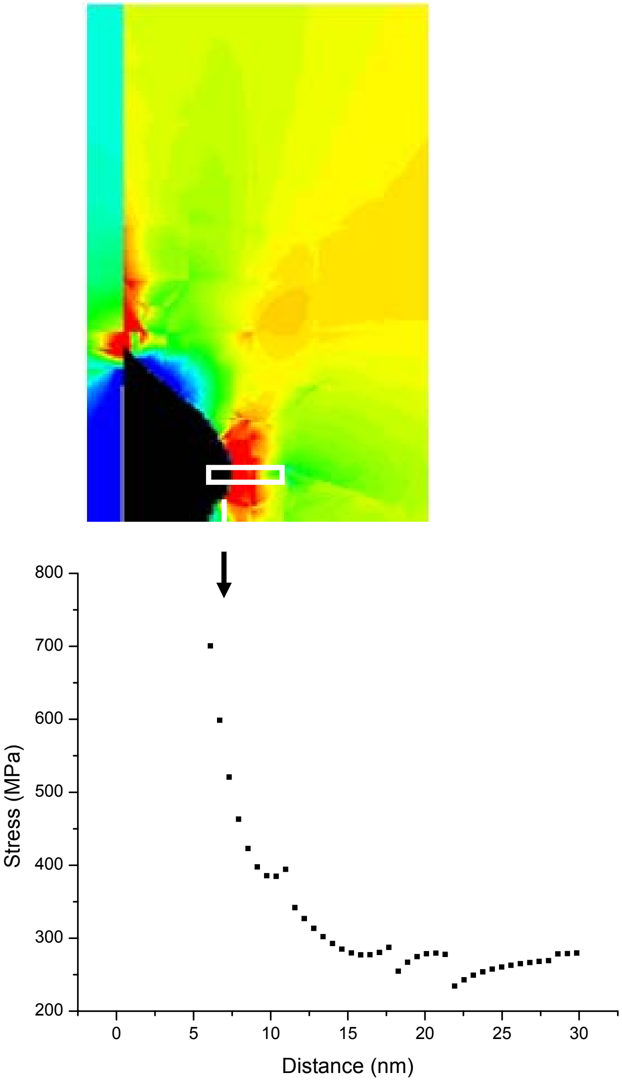

Fig. 4. 25: Local stress distribution at the tip of the void (in white box) in 180nm Cu interconnects

4.6 *IN-SITU STEM HEATING*

The effects of thickness contrast in HAADF STEM mode can be seen in Fig. 4.26 The right side of the TEM sample is near the vacuum. Since the sample is a plan view sample prepared by ion milling, the edge is wedge shaped. Thus there is an increase in thickness from right to left. A corresponding increase in brightness from right to left is also observed. This change in brightness is due to an increase in thickness. The following quantitative thickness measurements were made.

In order to solve equations (3.1-3.3.), the values listed in Table 4.1 were used. First, the characteristic scattering angle was calculated as

$$\theta_0 = \frac{0.117 Z^{1/3}}{E^{1/2}} = \frac{0.117 \times 29^{1/2}}{200^{1/2}} = 77.75 mrad \tag{4.2}$$

which was used to determine the elastic scattering cross-section, $\sigma(\beta) = 3.48 \times 10^{-22}$.
This value was then used to calculated the total elastic scattering cross section

$$Q_t = \frac{6.022 \times 10^{23} \times 3.48 \times 10^{-22} \times 8920 kg/m^3}{63.546 \times 10^{-3} kg/mol} = 2.942 \times 10^7 m^{-1} \tag{4.3}$$

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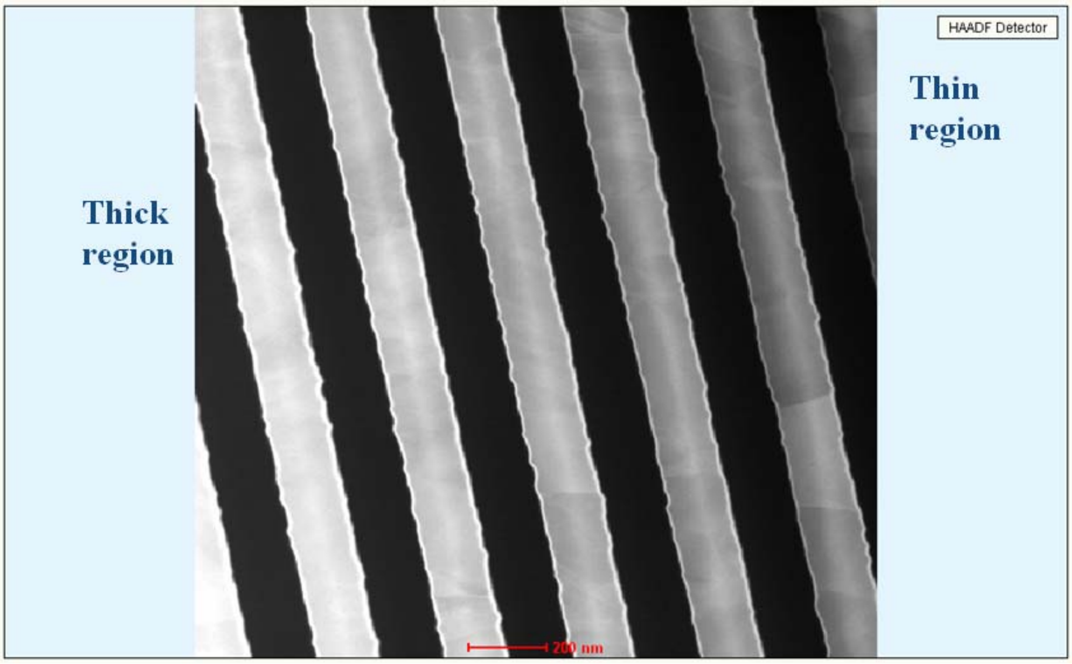


Fig. 4. 264: HAADF STEM image of planar 180 nm Cu interconnects TEM sample. The right side in the image is near vacuum, therefore thinner, while an increase in thickness occurs towards the right side of the image. As a result, an increase in intensity can be seen for an increasing thickness.

Table 4. 1: Table of values used to calculate total elastic scattering cross section.

Symbol	**Value**
Z	29
a_0	5.29×10^{-11} m
E	200keV
E_0	511keV
β	10mrad
N_0	6.022×10^{23} /mol
ρ	8920 kg m^{-3}
A	63.546 g/mol

This series of calculations allowed us to determine variations in contrast with changes in thickness during in-STEM heating experiments of void growth. Fig. 4.27 shows a HAADF STEM image of a full void, captured from a video sequence. Adjacent to the bottom region of the void, an area of bright contrast can be seen, while further down the intensity is considerably lower. Using the Gatan Digital Micrograph software, brightness values were obtained for the two regions (labeled A and B in Fig. 4.27) (grayscale TIFF image), for which a difference of approximately 42 (102 for bright, 60 for dark) was measured. Inserting these values into equation (3.1) gives

$$\frac{\Delta I}{I} = \frac{42}{60} = 2.942 \times 10^{7}\,\Delta t \tag{4.3}$$

which corresponds to a change in thickness of $\Delta t = 23.7nm$. Since the initial thickness of the sample was assumed to be about 50 nm, this means that upon formation of a complete void, the thickness of the adjacent line has increased by nearly 50%. This indicates that a considerable pileup of Cu material has occurred on the Cu surface near the Cu void.

A different experiment was performed, where void nucleation and growth was observed in real time (over a period of 4 minutes and 40 seconds) in HAADF STEM mode (Fig. 4.28). Although the images are not very clear due to the fact that they

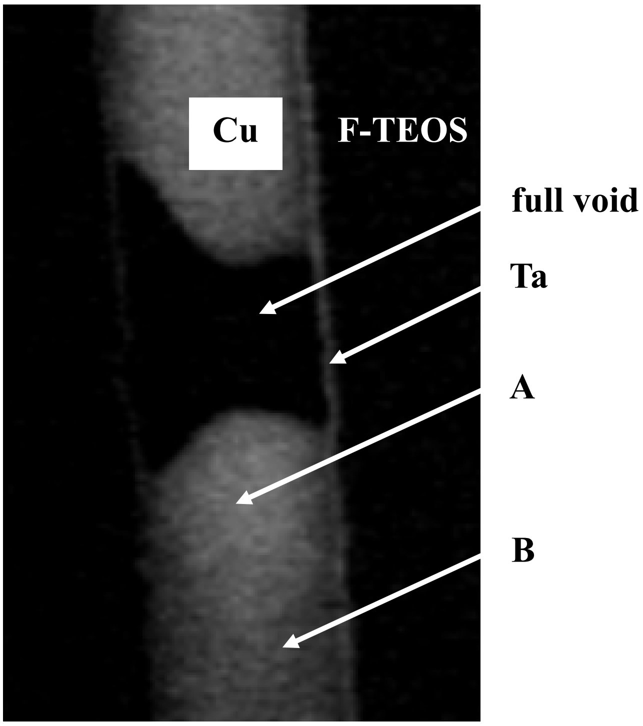


Fig. 4. 275: Figure shows a captured STEM image post void formation. The areas near the void (labeled ‘A’) are clearly brighter than regions further away (labeled ‘B’).

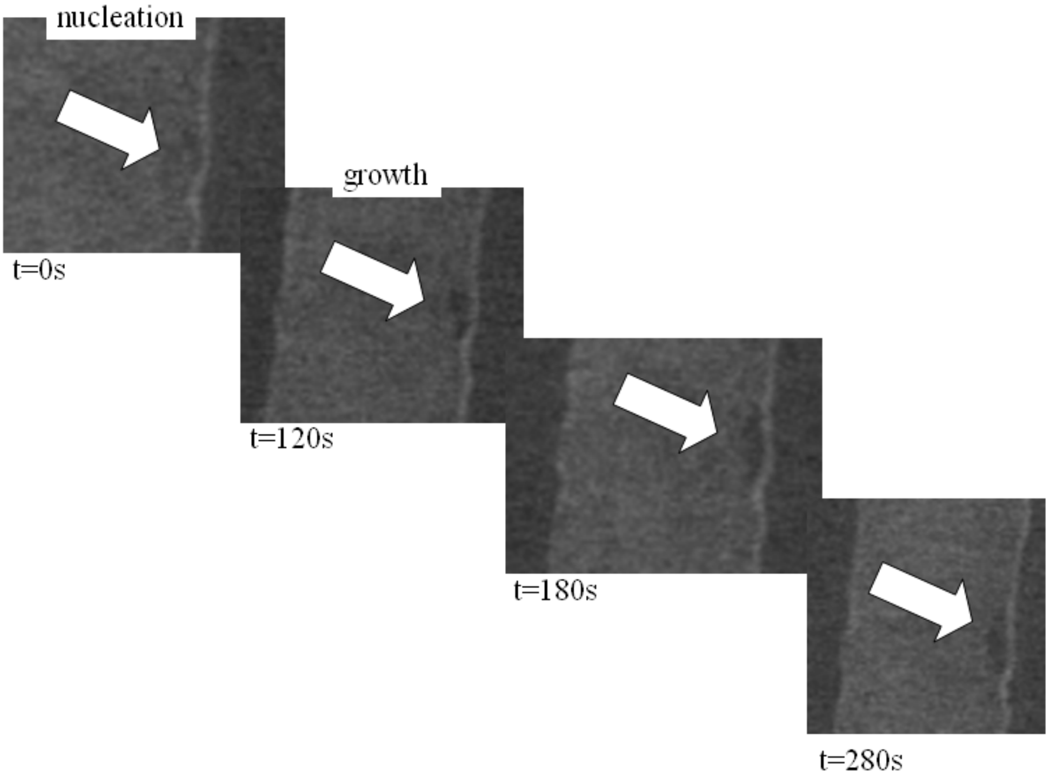


Fig. 4. 28: Void growth in HAADF STEM mode as a function of time.

were captured from a live video, no clear change in brightness could be identified. Fig. 4.29 shows the BF image of the same void, post void formation.

Another HAADF STEM image, this time with a higher resolution, from a void that formed in the middle of the line (corresponding BF TEM image is shown in Fig. 4.7), shows regions near the void with a significant dark contrast, which indicates a depletion of material. Using the Gatan Digital Micrograph software, brightness values were obtained for the two regions (labeled '**A'**-bright and '**B'**-dark in Fig. 4.30) (grayscale TIFF image), for which a difference of approximately 31 (84 for bright, 53 for dark) was measured. Calculations of the change in thickness at the dark area according to equation (3.1) gives

$$\frac{\Delta I}{I} = -\frac{31}{84} = -2.942 \times 10^{7} \Delta t$$

which corresponds to a change in thickness of $\Delta t = -12.5 nm$. On the other hand, no noticeable increase in intensity (indicating any pileup of the material) was noted. These results need to be interpreted carefully, as grains can originally exhibit slight differences in contrast due to non-uniform ion milling during sample preparation leading to slight variations in thickness.

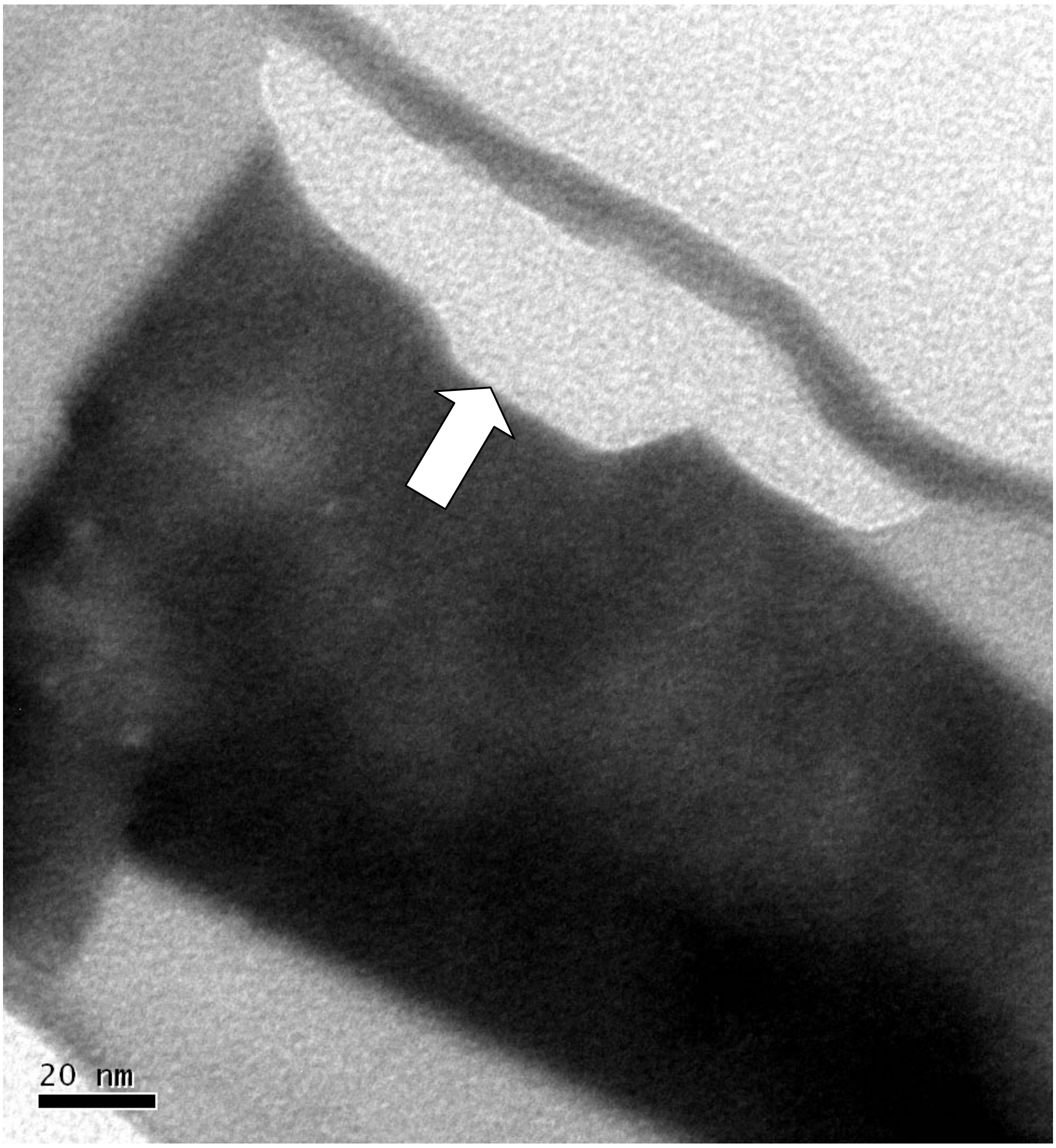


Fig. 4. 29: BF TEM image of void formed in Fig. 4.27. White arrow indicates a Cu grain boundary.

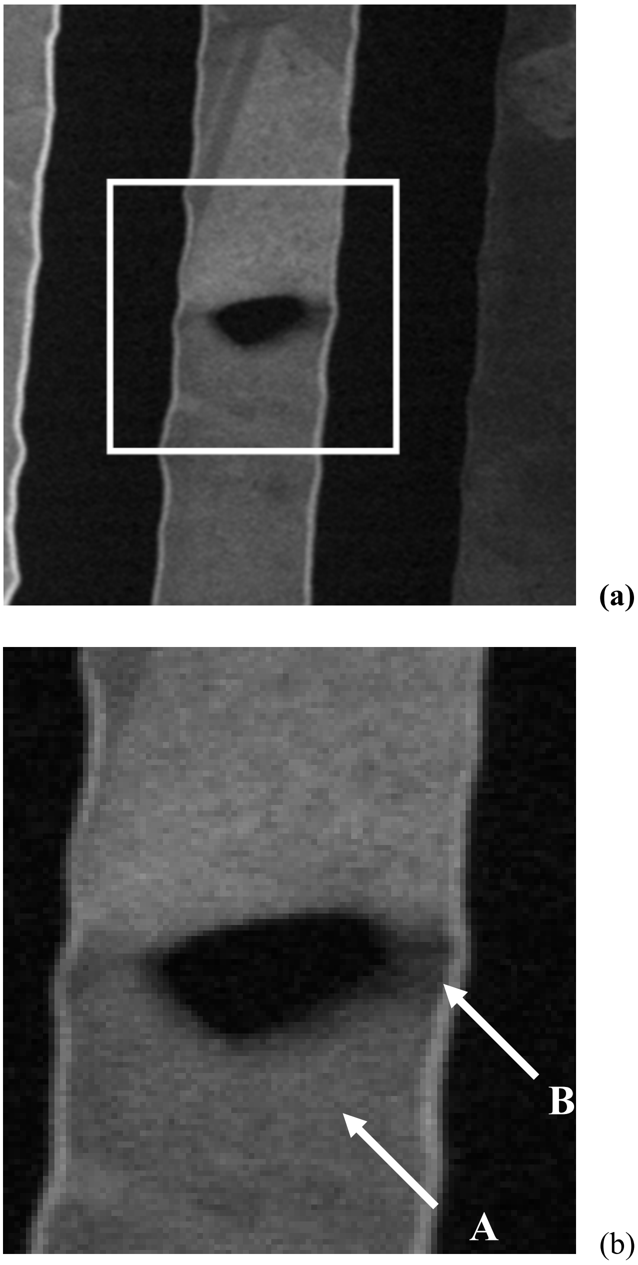


Fig. 4. 306: (a) HAADF STEM image of void in Fig. 4.7. (b) enlarged image of box in (a). Notice regions near the void (arrow) are darker in color indicating depletion of material.

CHAPTER 5: DISCUSSION

5.1 INFLUENCE OF CU INTERCONNECT LINEWIDTH ON STRESS RELAXATION BEHAVIOR

As discussed in Chapter 2, the state of stresses in Cu interconnects changes with dimensions of the metal layer. In particular, Cu thin films exhibit an isotropic biaxial state of stresses, whereas Cu passivated lines exhibit a triaxial state of stresses. As a result, the stress-temperature behavior for Cu thin films and passivated narrow lines is very different (Fig. 2.1 and Fig. 2.3). In the case of Cu thin films, the non-linear variation of stress as a function of temperature implies the existence of plastic deformation. On the other hand, narrow passivated lines exhibit a linear elastic response when subjected to a thermal treatment. Fig. 2.3 also shows that the triaxial stress state of passivated lines changes with line dimensions, namely σ_z increases as the line width/thickness ratio increases (lines get narrower for a given thickness).

This transition from plastic to elastic behavior was confirmed by *in-situ* TEM observations of 1.8 micron and 180 nm Cu interconnect lines, where nucleation of dislocations and void formation, respectively, were observed. In the case of the 1.8 micron lines, nucleation of dislocations at Cu grain boundaries was observed at 340°C during the 1st thermal cycle. Subsequent thermal cycles did not reveal additional dislocation motion. In addition, the role of the Cu/Ta DB interface on the stress relaxation mechanisms in 1.8 micron lines was better understood after *in-situ* TEM heating experiments. As shown in Fig. 4.5 the Cu/DB interface acts as a strong pinning barrier to dislocation motion. On the other hand, no voids were observed in the 1.8 micron lines. This does not mean necessarily that voids will never form in these structures, but likely much longer annealing times are required, as the *in-situ* TEM heating experiments carried out in this work were mostly done in under an hour. In fact, voids have been observed in Cu films under isotropic biaxial stresses [24].

In general, the nucleation and motion of dislocations in 1.8 micron lines during the 1st thermal cycle shows that Cu interconnects with wide linewidths are more likely, at least initially, to relax the stress through dislocation dynamics rather than void formation. This stress relaxation behavior of 1.8 micron lines is probably due to 1) the biaxial stress state of wide Cu lines, where shear stresses are predominant. This is a consequence of the fact that the thickness/width ratio for the 1.8 micron lines is 0.16, for which σ_z is very low (Fig. 2.3). 2) The local thermal activation of dislocations, which is diffusion related, and 3) the presence of high-angle boundaries, which are common in equiaxed grain structures and prone to the nucleation of dislocations.

For the 180 nm lines, despite the prior presence of dislocations, no dislocation nucleation and motion was observed during *in-situ* heating. This is due to the predominance of quasi-hydrostatic stresses (negligible shear stresses) in the lines, and the existence of a bamboo grain structure, with typical low energy grain boundaries, such as twin boundaries. The absence of any dislocation dynamics can be further understood by looking at the deviatoric stresses calculated based on OOF2 simulations. As was presented in Chapter 4.5, the deviatoric stresses were on the order of only a few MPa. This indicates that any dislocation motions is unlikely. Thus as the state of stresses is mainly hydrostatic, the stress is relaxed through the nucleation of voids by stress-assisted diffusion, rather through a dislocation mechanism. However, similar to the 1.8 micron lines, dislocations pinned at the Cu/DB interface showed jerky motion under the influence of temperature. This again shows the important role of this interface as a dislocation pinning barrier, unlike the Cu/SiN_x interface, which typically acts as a dislocation sink [50].

In this work, voids were observed to form between 220-250^{o}C during the first cycle. This range of temperatures seems to be higher than what was previously reported for void formation in Al (around 170^{o}C) [27] and slightly higher than what Ogawa *et. al.* [25] predicted for maximum voiding rate at 190^{o}C. It is important to bear in mind that these 180 nm lines, before being subjected to *in-situ* heating, are initially in a state of high tensile stresses [37] due to the fabrication process. Thus, as the temperature is increased, the stresses relax but diffusion is enhanced. The range of temperatures between 220 and 250 ^{o}C seems to be a compromise between sufficiently high hydrostatic stresses and significant diffusion, which allows voids to nucleate.

In all cases observed (more than 100), with one exception, voids nucleated at triple point junctions, where a Cu grain boundary terminates at the Ta diffusion barrier (Fig. 4.6). Void propagation was also monitored by *in-situ* TEM, as shown by the sequence of images taken over a 12 minute period (Fig. 4.9). In this case, the propagation of the void continued up to the point of failure. Clearly, grain A was consumed, whereas grain B seemed to act as a barrier during void growth. As the void propagated, it assumed a specific angle along most of the void length until total failure occurs. Most likely, this is due to the presence of low surface energy planes, which open up during void nucleation. These low energy planes exhibit high surface diffusion rates and thus, facilitated the propagation of the void. However, void propagation characteristics may not be determined by energetics alone. It is likely to be a balance between minimization of the surface energy and stress-assisted diffusion through the Cu/SiN_x interface and the Cu free surface.

These *in-situ* TEM experiments clearly show a definitive difference in the mode by which the stress relaxation operates in Cu interconnect lines with distinct thickness-to-width ratios. The results indicate that for smaller linewidths, the elastic response due to the quasi-hydrostatic state (negligible shear stress) leads to void formation through stress-assisted diffusion, rather than through dislocation nucleation and glide. The knowledge acquired in this work will become increasingly important to the future of microelectronics in which devices with dimensions below 100 nm will be commonplace.

5.2 FACTORS AFFECTING VOID FORMATION

According to the experimental results obtained (section 4.3), more that 100 voids were observed to nucleate preferentially at triple junctions where a Cu grain boundary meets the Ta DB. Only in one case, a void was observed to form in the middle of the Cu lines. A more detailed observation of void nucleation was carried out in three separate experiments, where a total of 47 triple junctions were present. In two of these experiments, the voids were observed to form in regions of high local stresses and high stress gradients (Fig. 4.19, Fig. 4.23). On the other hand, in the remaining experiment, the void formed in a region where the local stresses and the stress gradients were low (Fig. 4.21).

In this context, there are two questions that must be addressed: 1) Why do voids nucleate preferentially at triple junctions where a Cu grain boundary meets the Ta DB? and 2) Among the possible triple junctions nucleation sites, why do voids nucleate in specific locations?

In order to answer these questions and understand void formation in Cu interconnects, we should consider the following possible effects, namely 1) the energetics of the interfaces present, 2) grain orientation/local stresses, 3) stress gradients, 4) available vacancy diffusion paths and 5) concentration of defects.

5.2.1 Role of interfaces

Let us start by looking into the role played by the various interfaces on the formation of voids. The energetics and nucleation rate of void formation was considered by Gleixner and Nix for the case of Al [21], who concluded that vacancy condensation was not expected in Al interconnect lines. Instead, these authors claimed that void formation occurred due to the presence of defects at the Al/Al_2O_3 interface. These authors also suggested that although the density of defects is uniform along the Al/Al_2O_3 interfaces, voids nucleate at triple junctions due to fast grain boundary diffusion paths available for vacancy diffusion (as opposed to bulk diffusion).

In this thesis work, voids are also observed to nucleate at triple junctions, particularly where a Cu grain boundary meets the Ta diffusion barrier (Fig. 5.1(a)). For Cu, the aforementioned argument of voids forming due to the presence of defects is less convincing because Cu and Ta are known to form a DB interface with very strong adhesion. Therefore, in order to explain the preferential void formation at triple junctions, the energy of the various interfaces present will be examined next.

For the calculations, three different possible void formation sites are considered (Fig. 5.1): (a) triple junction (model I), (b) Cu/DB interface (model II), and (c) Cu grain boundary (model III). In general, the change in Helmholtz free energy due to void formation can be expressed as

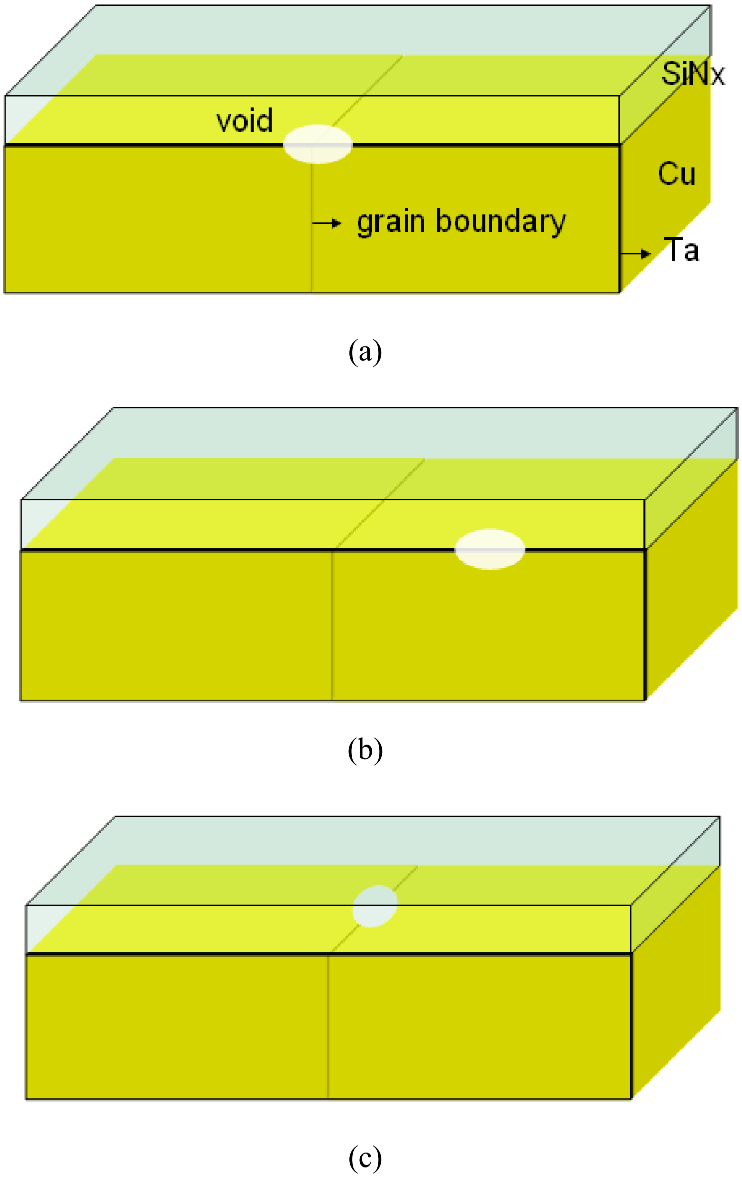


Fig. 5.1: (a) Quarter sphere void nucleates at Cu/DB triple junction (model I) (b) Quarter sphere void nucleates at Cu/DB interface away from the triple junction (model II) (c) Half sphere void nucleates at Cu grain boundary away from the Cu/DB interface (model III).

$$\Delta F = \Delta F_{el} V + \sum \gamma_{free} A_{free} - \sum \gamma_{interface} A_{interface} \tag{5.1}$$

where ΔF_{el} is the change in free energy per unit volume, V the volume of the void, $\sum \gamma_{free} A_{free}$ the total increase in free energy (γ_{free}) due to the creation of new surfaces with area A_{free}, and $\sum \gamma_{interface} A_{interface}$ the reduction in interfacial free energy ($\gamma_{interface}$) due to the destruction of interfacial area ($A_{interface}$).

Starting with model I, where the nucleation of voids occurs at triple junctions located at the Cu/Ta diffusion barrier (Fig. 5.1 (a)), we assume the void to be a quarter sphere of radius *r* (Fig. 5.2). In addition, as the TEM Cu interconnect samples observed in this work are passivated at the top surface and unpassivated at the bottom surface we need to consider these two possible locations. Assuming first the case where the SiN_x passivation layer is present, the following new surfaces will be created upon nucleation of a void: Cu free surface with an area $A_{Cu\text{-}free} = \frac{1}{4} \times 4\pi r^2$, SiN_x free surface with an area $A_{SiNx\text{-}free} = \frac{1}{2} \times \pi r^2$ and Ta free surface with an area $A_{Ta\text{-}free} = \frac{1}{2} \times \pi r^2$. On the other hand, the following interfaces will be eliminated: Cu grain boundary with an area $A_{gb} = \frac{1}{4} \times \pi r^2$, Cu/Ta interface with an area $A_{Cu\text{-}Ta} = \frac{1}{2} \times \pi r^2$ and

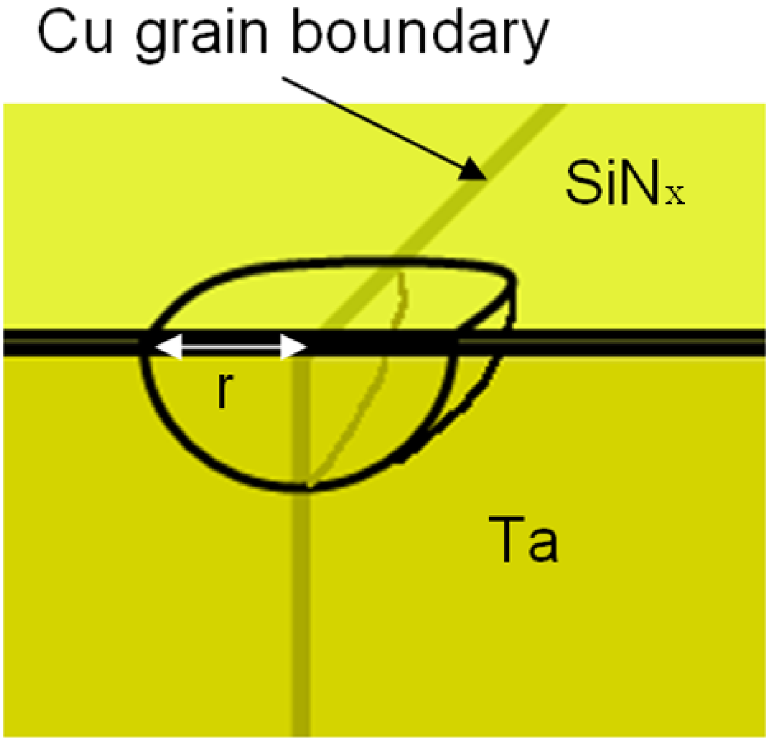


Fig. 5. 2: Quarter sphere void with radius r nucleating at the Cu/Ta diffusion barrier interface-Cu grain boundary triple junction.

Cu/SiN$_x$ interface with an area A$_{\text{Cu-SiNx}}$ $=\frac{1}{2}\times\pi r^2$. Thus, for a void of volume V$=\frac{1}{4}\times\frac{4}{3}\pi r^3$, equation (5.1) can be expanded to give

$$\Delta F = \frac{1}{3}\pi r^3 \Delta F_{el} + \frac{1}{2}\pi r^2 \gamma_{SiNx-free} + \frac{1}{2}\pi r^2 \gamma_{Ta-free} + \frac{1}{4}4\pi r^2 \gamma_{Cu-free}$$

$$-\frac{1}{4}\pi r^2 \gamma_{gb} - \frac{1}{2}\pi r^2 \gamma_{Cu-SiNx} - \frac{1}{2}\pi r^2 \gamma_{Cu-Ta} \qquad (5.2)$$

where $\gamma_{SiNx-free}$ is the SiN$_x$ free surface energy, $\gamma_{Ta-free}$ the Ta free surface energy, γ_{gb} the Cu grain boundary energy, $\gamma_{Cu-SiNx}$ the Cu/SiN$_x$ interfacial energy, and γ_{Cu-Ta} the Cu/Ta interfacial energy.

According to equation (5.2), the free energy function increases with radius *r* up to a critical radius where it reaches a maximum value, followed by a monotonic decrease with increasing *r*. The void critical radius, r* which represents the void size above which voids are stable and able to grow, can be obtained through the expression

$$\frac{\partial \Delta F}{\partial r} = \pi r^2 \Delta F_{el} + 2\pi r\left(\frac{1}{2}\gamma_{SiNx-free} + \frac{1}{2}\gamma_{Ta-free} + \gamma_{Cu-free}\right)$$

$$+ 2\pi r\left(-\frac{1}{4}\gamma_{gb} - \frac{1}{2}\gamma_{Cu-SiNx} - \frac{1}{2}\gamma_{Cu-Ta}\right) = 0 \qquad (5.3)$$

which has the following solution:

$$r^* = \frac{2\left(\frac{1}{2}\gamma_{SiNx-free} + \frac{1}{2}\gamma_{Ta-free} + \gamma_{Cu-free} - \frac{1}{4}\gamma_{gb} - \frac{1}{2}\gamma_{Cu-SiNx} - \frac{1}{2}\gamma_{Cu-Ta}\right)}{\Delta F_{el}} = \frac{2\sum\gamma^I}{\Delta F_{el}} \qquad (5.4)$$

$\sum\gamma^I$ denotes the summation of all the surface/interface energy terms for model I. Assuming the coalescence of vacancies in a material under stress, then $\Delta F_{el} = -\sigma$. As from the OOF2 simulations, the range of local hydrostatic stresses found in 180 nm Cu interconnects varied from around 300 MPa to slightly over 400 MPa (see section 4.5), we use the highest stress of 400 MPa to calculate r*, as this minimizes the critical radius. To account for the surface energy terms we use the values available in the open literature (Table 5.1). As the surface energy values reported/calculated exhibit a considerable range (e.g. the Cu-Ta interfacial energy ranges within an order of magnitude), a minimum possible summation ($\sum\gamma^I_{\min}$) and a maximum possible summation ($\sum\gamma^I_{\max}$) (Table 5.2) of all surface/interfacial energies

Table 5. 1 : Energy values used for calculating change in free energy for void formation.

	Energy (J/m^2)	Reference
Cu grain boundary	0.3-0.95	92
Cu-SiN$_x$ interface	0.9-2.2	93
Cu-Ta interface	0.18-1.31	94
Surface energy of Cu	1.41- 2.31	95-96
Ta surface energy	1.79-3.45	97
SiN$_x$ surface energy	1.2	98

Table 5. 2: Minimum and maximum summation of free surface and interface energies each model case.

A range of 1.46 to 4.77 J/m^2 can be found.

	Cu/Ta/Cu g.b. triple Junction		Cu/Ta with no g.b.		Middle of g.b.	
	Cu-SiN_x	Cu	Cu-SiN_x	Cu	Cu-SiN_x	Cu
$\sum \gamma_{max}$	4.02	3.87	4.10	3.95	4.77	2.11
$\sum \gamma_{min}$	1.46	1.96	1.70	2.20	2.45	1.49

will be used to estimate the upper and lower bounds for the critical radius (Table 5.3). For an hydrostatic stress of 400 MPa, the lower and upper bound critical radii were found to be

$r^*_{\max} = 20.01nm$ for $\sum \gamma^I_{\min}$ $(\sigma = 400MPa)$

$r^*_{\min} = 7.30nm$ for $\sum \gamma^I_{\max}$ $(\sigma = 400MPa)$

Although a hydrostatic stress of 400 MPa was found from the OOF2 calculations, the actual value of stress present in the experiments reported herein requires some further discussion. This is because in the OOF2 calculations, only σ_x and σ_y were used as boundary conditions [37], while σ_z =86MPa was neglected due to the 2-D nature of the OOF2 software. If 3-D simulations were performed, the hydrostatic stress would likely be higher. In addition, the stresses in thin TEM samples are different from those for real interconnects, a point which was discussed in Chapter 3. In fact, an increase of 1.7 to 1.8 times the original stresses should be present in the TEM samples. When these factors are taken into account, is not unreasonable to consider an upper level stress of 1GPa. Thus, for $\Delta F_{el} = -1GPa$, the lower and upper bound void critical radii can be calculated as

$r^*_{\max} = 8.04nm$ for $\sum \gamma^I_{\min}$ $(\sigma = 1GPa)$

Table 5.3: Critical radius (nm) for void formation for minimum and maximum range of surface energies.

Hydrostatic stress values of 400 MPa and 1 GPa were used.

	Hydrostatic Stresses	Cu/Ta/Cu g.b. triple Junction		Cu/Ta with no g.b.		Middle of g.b.	
		Cu-SiN$_x$	Cu	Cu-SiN$_x$	Cu	Cu-SiN$_x$	Cu
$\sum \gamma_{max}$	400 MPa	20.01	19.35	20.50	19.75	11.93	10.55
	1 Gpa	8.04	7.74	8.20	7.90	4.77	4.22
$\sum \gamma_{min}$	400 MPa	7.30	9.80	8.50	11.00	6.13	7.45
	1 Gpa	2.92	3.92	3.40	4.40	2.45	2.98

$r^*_{\min} = 2.92nm$ for $\sum \gamma^I_{\max}$ $(\sigma = 1GPa)$

In general, the range of possible critical radii as a function of stress according to model I can be more easily observed in Figs. 5.3 and 5.4 for which the $\sum \gamma^I_{\min}$ and $\sum \gamma^I_{\max}$ conditions are considered. The results for models II and III can also be observed in Figs. 5.3 and 5.4, but will be discussed later.

Once the critical radius is determined, the activation free energy ΔF^* for void nucleation can be calculated by inserting r* in for *r* into equation (5.2) which gives ΔF^*.

$$\begin{aligned}
\Delta F^* &= \frac{1}{3}\pi (r^*)^3 \Delta F_{el} + \frac{1}{2}\pi (r^*)^2 \gamma_{SiNx-free} + \frac{1}{2}\pi (r^*)^2 \gamma_{Ta-free} + \frac{1}{4} 4\pi (r^*)^2 \gamma_{Cu-free} \\
&\quad - \frac{1}{4}\pi (r^*)^2 \gamma_{gb} - \frac{1}{2}\pi (r^*)^2 \gamma_{Cu-SiNx} - \frac{1}{2}\pi (r^*)^2 \gamma_{Cu-Ta} \\
&= \frac{20\pi}{3} \frac{\left(\sum \gamma^I\right)^3}{\Delta F_{el}^{\ 2}} \qquad (5.5)
\end{aligned}$$

In this fashion, we can plot ΔF^* as a function of stress, as shown in Figs. 5.5 and 5.6. It is evident that the activation energy is much too large for voids to nucleate through this process, even for a hypothetical stress of 2 GPa.

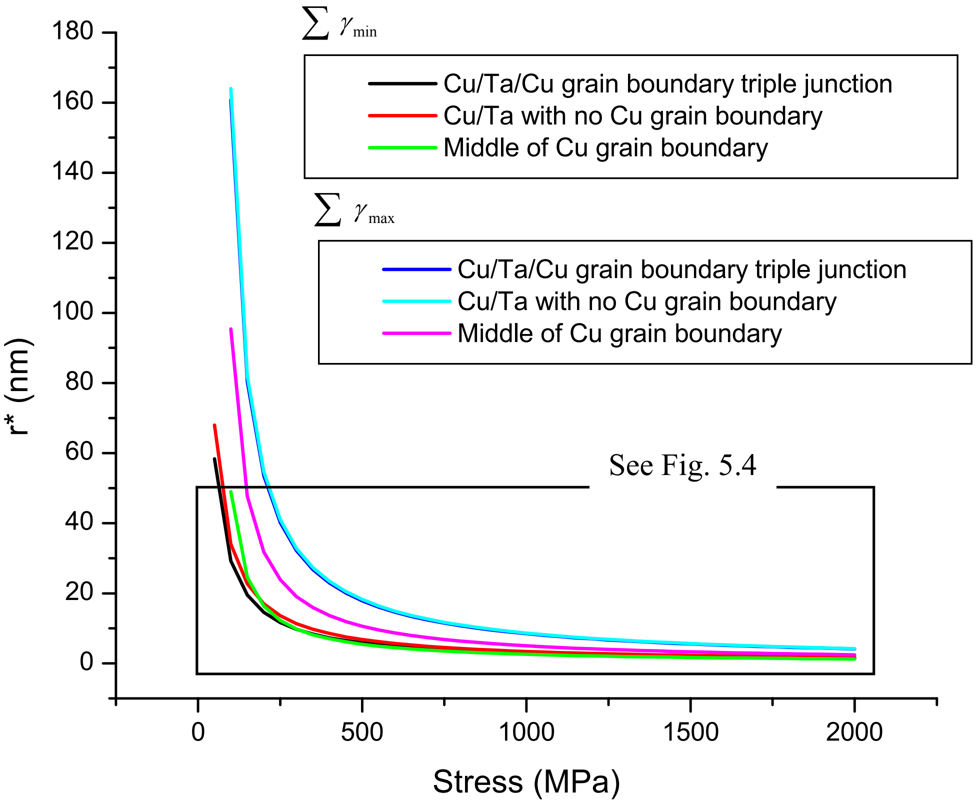


Fig. 5.3: Critical radius (r*) for void formation as a function of stress for the maximum and minimum summation of $\sum \gamma$ for the 3 possible void nucleation sites. Box inset on following page (Fig. 5.4).

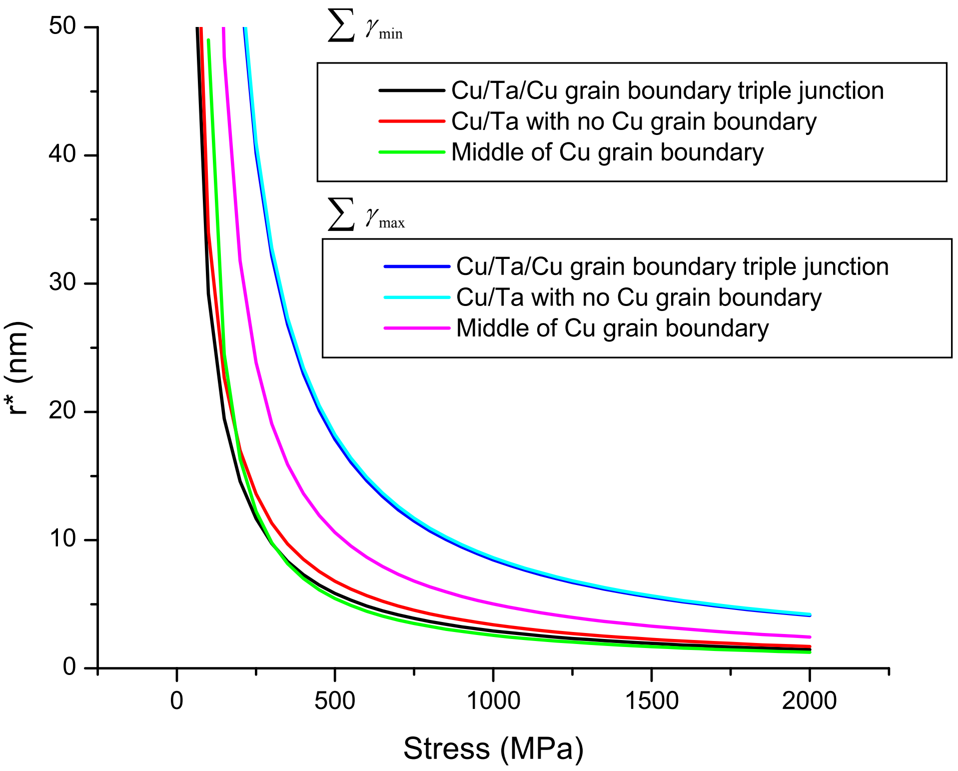


Fig. 5.4: Fig. 5.3 rescaled for the critical radius as a function of stress for the maximum and minimum summation of $\sum \gamma$ for the 3 possible void nucleation sites.

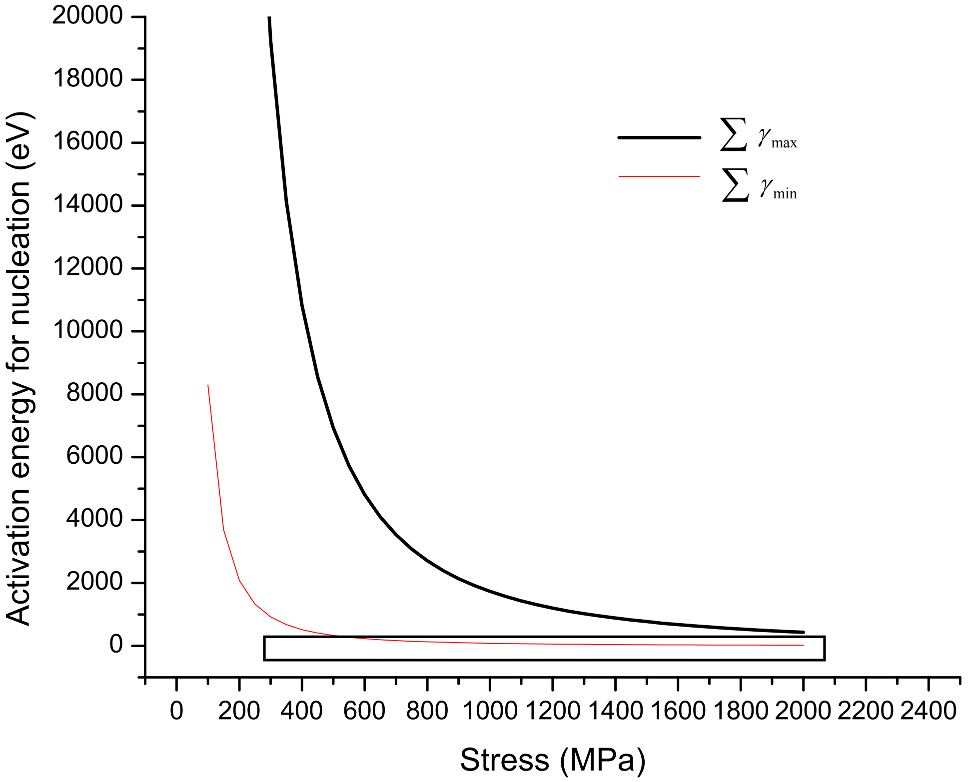


Fig. 5. 5 : Change in activation energy as a function of stress for a void nucleating at the triple junction on the CU/SiN$_x$ interface. Box inset on following page (Fig. 5.6).

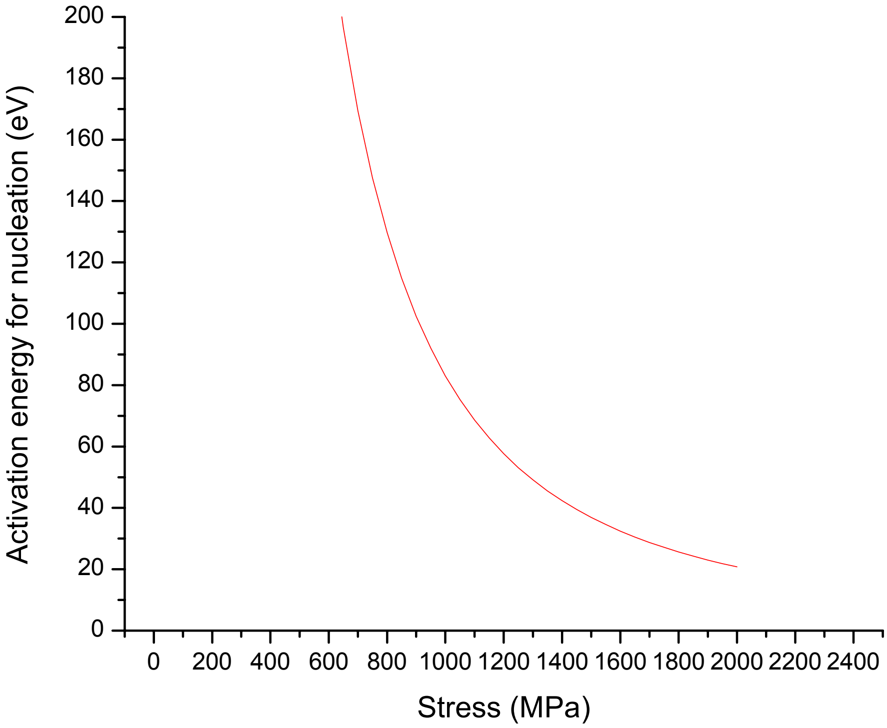


Fig. 5.6: Activation energy values for $\sum \gamma_{\min}$ at triple junction as a function of stress.

Now let’s consider model II where a quarter sphere void nucleates at the Cu/Ta interface away from a grain boundary (Fig. 5.1(b)). In this case, the change in Helmholtz free energy due to void formation is similar to model I, with the exception that for model II, the Cu grain boundary does not play any role. Therefore, equation (5.2) can be rewritten in the form

$$\Delta F = \frac{1}{3}\pi r^3 \Delta F_{el} + \frac{1}{2}\pi r^2 \gamma_{SiNx-free} + \frac{1}{2}\pi r^2 \gamma_{Ta-free} + \frac{1}{4}4\pi r^2 \gamma_{Cu-free}$$

$$- \frac{1}{2}\pi r^2 \gamma_{Cu-SiNx} - \frac{1}{2}\pi r^2 \gamma_{Cu-Ta} \tag{5.6}$$

where all the terms have the same meaning as before. Using the same procedure, the critical radius can be determined by solving $\frac{\partial \Delta F}{\partial r} = 0$, which gives

$$r^* = \frac{2\left(\frac{1}{2}\gamma_{SiNx-free} + \frac{1}{2}\gamma_{Ta-free} + \gamma_{Cu-free} - \frac{1}{2}\gamma_{Cu-SiNx} - \frac{1}{2}\gamma_{Cu-Ta}\right)}{\Delta F_{el}} = \frac{2\sum\gamma^{II}}{\Delta F_{el}} \tag{5.7}$$

The results are shown in Figs 5.5 and 5.6 for $\sum\gamma^{II}_{\min}$ and $\sum\gamma^{II}_{\max}$. As compared to model I, there are no significant differences in the critical radius for a given stress value. As $\sum\gamma$ and the void critical radius does not vary significantly from model I,

ΔF^* is approximately the same for model II.

Model III considers the possibility of voids forming at the Cu grain boundary (Fig. 5.1(c)). For this case, we consider the void to be a half sphere of radius *r*. For model III, the change in Helmholtz free energy due to void formation is calculated by modifying equation (5.2) to address the absence of the Ta DB. Thus, equation (5.2) becomes

$$\Delta F = \frac{2}{3}\pi r^3 \Delta F_{el} + \pi r^2 \gamma_{SiNx-free} + \frac{1}{2} 4\pi r^2 \gamma_{Cu-free} - \pi r^2 \gamma_{Cu-SiNx} - \frac{1}{2}\pi r^2 \gamma_{gb} \qquad (5.8)$$

As before, to determine the critical radius, we solve $\frac{\partial \Delta F}{\partial r} = 0$, which gives

$$r^* = \frac{\left(\gamma_{SiNx-free} + 2\gamma_{Cu-free} - \gamma_{Cu-SiNx} - \frac{1}{2}\gamma_{gb}\right)}{\Delta F_{el}} = \frac{\sum \gamma^{III}}{\Delta F_{el}} \qquad (5.9)$$

The changes in critical radius as a function of the stress is shown in Figs 5.3 and 5.4 for $\sum \gamma_{\min}^{III}$ and $\sum \gamma_{\max}^{III}$. As compared to model I or II, the critical radii r* are smaller for $\sum \gamma_{\max}^{III}$, but a significant difference is not seen. The maximum and minimum summation of $\sum \gamma^{III}$ is shown in Table 5.2.

As the r* and $\sum\gamma$ does not vary significantly from models I and II, ΔF^* is approximately the same for model III. Therefore, for models I, II and II, it seems unlikely that the energetics alone are responsible for void formation.

We are now left with the calculations for the case where the SiN_x passivation layer is absent at bottom surface, due to TEM sample preparation. This is important as the images obtained in by TEM are 2D projections, and in such a case, it is not possible to determine if voids nucleate at the top Cu/SiN_x interface or at the bottom Cu free surface.

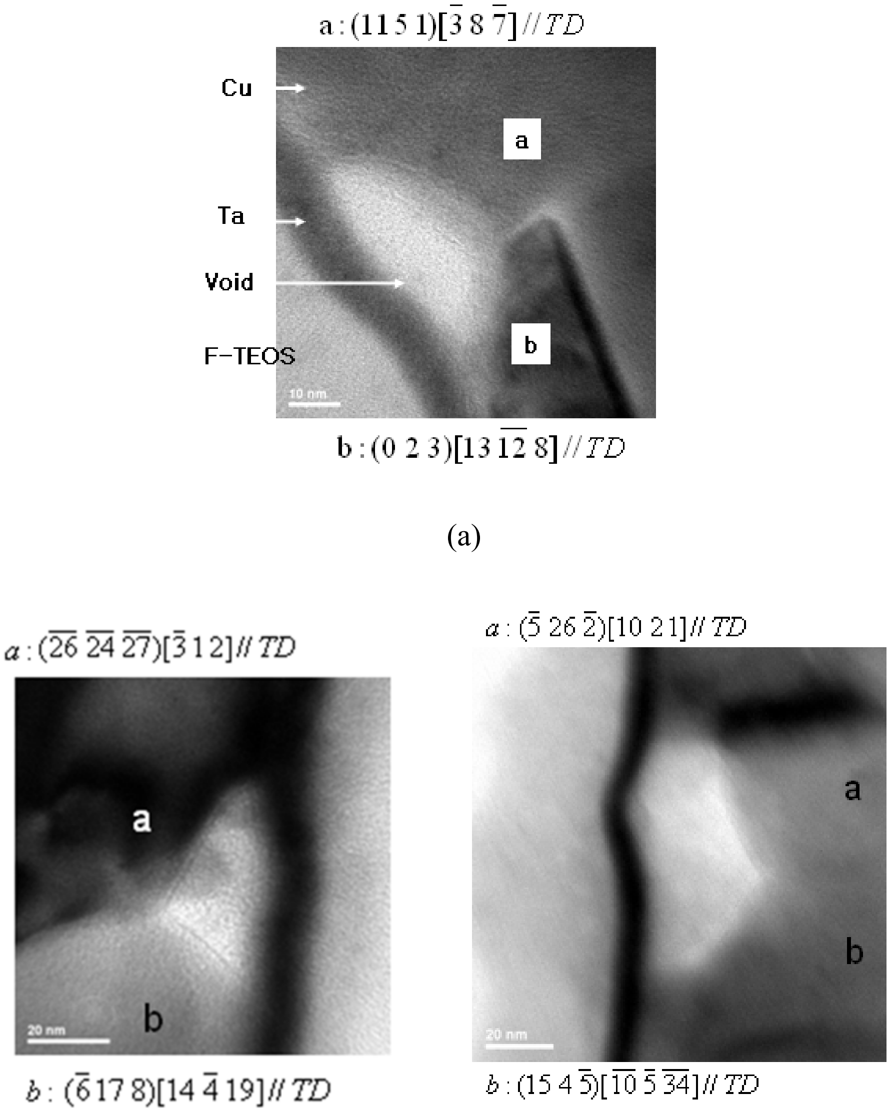
The summation of the minimum and maximum of the free/interfacial energies was given in Table 5.2 As it can be seen, the summation of the free/interfacial energies do not significantly change due to void formation at the Cu free surface. For example, the $\sum\gamma_{\min}^{I}$ for the void nucleating at both the Cu/SiN_x interface or Cu free surface have values of 1.46 and 1.96 J/m^2. Likewise, the corresponding r* for each case is 2.92 and 3.92 nm respectively. As such, the critical radius for void formation at the Cu free surface, for models I, II or III, will not affect the critical energy significantly. Hence it can be concluded that void formation at the triple junctions is not solely due to the energetics of the interfaces. As will be discussed in section 5.2.4, the presence of defects cannot be ruled out. In particular, the presence of contaminants in the electroplating bath (e.g. sulfuric acid, chlorides [77]), copper oxide formation, or other defects could significantly alter the energetics for void nucleation. In addition, the energetics of void nucleation might be better understood if there was a better understanding of the Cu/Ta interfacial energies as was seen in Table 5.1. This understanding of the specific interfacial energies at the Cu/Ta interface, as well as the understanding of the types and density of defects could also be important in understanding the mechanisms for void nucleation.

5.2.2 Role of grain orientation/diffusion paths

From the previous section we learned that the energies of the interfaces present are not likely to control the nucleation of voids. Therefore, the fact that voids seem to nucleate preferentially at triple junctions where a Cu grain boundary meets the DB still needs to be explained. In this regard, one aspect to consider is the overall number of available triple junctions at the Cu/DB interface and within the Cu lines. A simple count reveals that triple junctions at the Cu/DB interface are a factor of three higher than within the Cu lines.

Therefore, the higher number of triple junctions at the Cu/DB interface increases the probability of void nucleation at these sites. But, why are triple junction preferred sites? To answer this question, we should look first at the misorientation between grains. For a general scenario where there is a significant misorientation (> 10^o) between grains, the triple junctions are points of high local stress. This in turn promotes the formation of stress gradients. Furthermore, as three interfaces converge at triple junctions and high-angle boundaries provide fast diffusion paths through the grain boundaries, it seems that all the conditions are met to drive vacancies to triple junctions and initiate void formation. Additionally, since these three interfaces exhibit different diffusivities, there should be a significant flux divergence at these triple junctions. These conditions are ideal for nucleation to occur at triple junctions. This mechanism can explain why voids do not form at the Cu/Ta interface away from a grain boundary, as these regions lack the high local stresses (based on the simulated local stress results) and fast diffusion paths through high-angle boundaries. In addition, the flux divergence will not be as significant due to the absence of grain boundaries with high diffusivities.

We should now turn to the discussion to the *in-situ* TEM observations that show that while triple junctions are the preferred sites for void formation, the location of these sites is very specific. In fact, during the experiments, while many triple junctions were available, void formation occurred in particular locations. To learn more about these specific locations, grain orientation analysis was conducted in the regions where voids were observed to form. In the first experiment, the void formed at a triple junction where two grains with orientations (11 5 1) and (0 2 3) met at the Cu/Ta DB interface (Fig.5.7a). These grains have a misorientation angle of 10.37^{o}. In the second experiment, the void formed at a triple junction where two grains with orientation $(\bar{6}\,17\,8)$ and $(\overline{26}\,\overline{24}\,\overline{27})$ and misorientation angle of 24.84^{o} met at the Cu/Ta DB interface (Fig.5.7b). Finally, the third void formed at a triple junction



(a)

(b) (c)

Fig. 5.7 : TEM of void from Chapter 4. (a)-(c) shows three different voids observed to form during in-situ TEM heating experiments. The crystal orientation of the grains adjacent to the voids are shown.

where two grains with orientations $(\bar{5}\ 26\ \bar{2})$ and $(15\ 4\ \bar{5})$ and a misorientation angle of 14.1^{o} meet at the Cu/Ta DB interface (Fig.5.7c).

These results show that in all three cases, the misorientation angles were all higher than $10\ ^{o}$. Nucci *et. al.* [66] reported earlier that such high angle grain boundaries promote the formation of voids to reduce their high energy. However, as previously discussed in section 5.2.1, the grain boundary energy does not seem to be controlling the formation of the voids. Therefore, an alternative explanation for the role of grain boundaries is to consider the fast diffusion paths provided by high-angle boundaries, which can facilitate void formation. An additional consequence of large misorientations between Cu grains is the presence of high local stresses and steep stress gradients. This will be discussed next.

5.2.3 Role of local stresses/stress gradients

Due to the misorientation between Cu grains and the anisotropic character of Cu, local stresses develop in Cu interconnects. Therefore it is important to correlate the presence of local stresses with void formation. Among the three experiments carried out, two of these show the formation of voids in regions of high local stresses and high stress gradients (Fig 4.18, 4.22). On the other hand, the remaining experiment shows the formation of a void in a region where the local stresses and the stress gradients were low (Fig 4.20). In particular, in the first experiment (Fig 4.18), void formation occurred at the site of maximum local stresses, whereas in the second experiment, the local stress at the void formation site, although not the highest, was still high. In the final experiment, however, the void formed at a triple junction which did not exhibit a very high local stress. Reasons for this behavior are not fully understood, although a few scenarios are possible. First, the range of stresses from point-to-point on the Cu interconnects lines does not vary by more than 100 MPa. Second, a precise correlation between the local stresses present and void formation should be made carefully, as only a 2D FEM stress simulation was performed. The inclusion of σ_z =85MPa could alter the magnitude of the absolute stresses. Third, perhaps the site in question had diffusion paths readily available.

In general, while being conservative at this point, it seems that there is a correlation between high local stresses and void formation.

Furthermore, in order to understand the changes in stress introduced by the formation of the void, stress simulations were carried out before and after void formation. Fig.4.23 shows that the local stresses increase significantly upon void formation, particularly at the corners of the void (Fig. 4.23), where hydrostatic stresses exceeding 600 MPa were calculated. These stresses are well over the maximum 430 MPa observed in Cu lines prior to void formation. In addition, steep stress gradients develop adjacent to the void, which provide a high driving force for void growth after the void nucleates.

5.2.4 Concentration of defects

Defects can exist in various forms in Cu interconnects, including vacancies, dislocations and interfacial flaws at the Cu/Ta interface. In addition, a high defect concentration is known to exist at the Cu/SiN$_x$ interface, due to the Chemical Mechanical Polishing (CMP) process after electroplating. Therefore, these defects can play a role in void formation.

Let us first consider the effects of vacancy concentration on void formation. The classic theory for determining the equilibrium concentration of vacancies as a function of temperature is given by [89] .

$$C = \exp\left(\frac{S_v^f}{k} - \frac{H_v^f}{kT} \right) \tag{5.4}$$

where, S_v^f is the entropy for single vacancy formation, H_v^f the enthalpy for single vacancy formation, k is Boltzmans constant and T is the temperature in K. For Cu, $S_v^f = 3.0 \pm 0.3k$ and $H_v^f = 1.19 \pm 0.03eV$ [89]. However under the influence of stress, the vacancy concentration increases, which can be expressed by [90];

$$C = \exp\left(\frac{S_v^f}{k} - \frac{H_v^f}{kT} \right) \exp\left(\frac{\sigma\Omega_v}{kT} \right) \tag{5.5}$$

where σ is the stress and Ω_v the vacancy volume. Assuming for Cu, $\Omega_v = 1.422 \times 10^{-30} m^3$ [91], the vacancy concentration was calculated over a temperature range of 50 to 500°C for various stress levels (Fig. 5.8). Since the voids observed in this work formed at temperatures between 220 °C and 250 °C, and the stress simulations were carried out at 230 °C, the vacancy concentration is compared at this temperature as a function of stress (Fig. 5.8 and Table 5.4). The results show that the effects of stress on vacancy concentration is not significant. In fact, at 1 GPa, the vacancy concentration is 3.07×10^{-11}, about 1.5 times the concentration under no stress. Nevertheless, points of high local stress, such as triple junctions should lead to higher vacancy concentrations. Keeping in mind the increased concentration of vacancies at triple junctions, is the condensation of these vacancies enough to explain the void sizes observed during *in-situ* TEM experiments? To address this question, let us consider the formation of voids at the Cu/Ta triple junction. According to Table 5.1, the critical radius for void formation is 2.92 nm at 1 GPa. As the number of vacancies necessary to produce a void radius of critical radius r* is given by [21];

$$n^* = \frac{V}{\Omega} \tag{5.4}$$

where Ω is the atomic volume = 11.80 Å^3 for Cu and $V = \frac{1}{4} \times \frac{4}{3} \pi r^3$ is the volume of

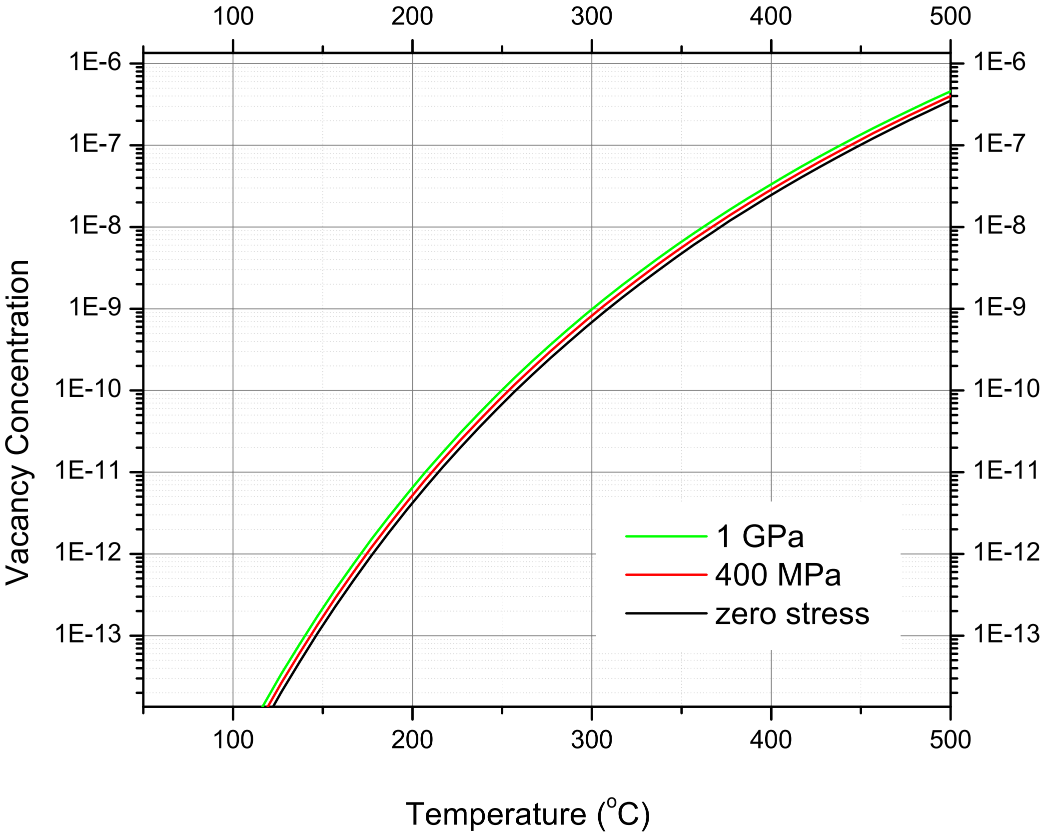


Fig. 5. 8: Equilibrium vacancy concentration as a function of temperature for zero stress, 400 MPa, and 1 GPa conditions.

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Table 5. 4 : Vacancy concentration as a function of stress at T=230°C.

Stress	No stress (equilibrium)	400 MPa	1 GPa
Vacancy Concentration	2.03×10^{-11}	2.49×10^{-11}	3.07×10^{-11}

a quarter sphere, thus for r*=3nm, $n^* \approx 2400$ vacancies. Taking into consideration the values for the concentration of vacancies at 230 °C, this means that the random statistical condensation of vacancies cannot explain the void size observed.

During the *in-situ* TEM observations reported in this work, the voids were seen to nucleate instantaneously. Therefore, if we assume the period of a ½ second for void formation, vacancies can travel a distance given by $x \sim \sqrt{Dt}$, where $D = D_o \exp(-\frac{Q}{kT})$ is the diffusion coefficient, D_0 is the pre-exponential factor, Q the activation energy, k Boltzmann's factor, T the temperature in K and t the time (s). The pre-exponential terms were calculated from table 5.5 [7], where δ is the grain boundary width, and T_m is the melting temperature. For the activation energies, the values given in Table 5.6 [7] were used, where ΔH_B, ΔH_{GB}, and ΔH_S are the activation energies for bulk, grain boundary, and surface respectively in eV/atom.

The diffusion coefficients as a function of temperature are shown in Fig. 5.9. From Fig. 5.9, the diffusion coefficients for bulk, grain boundary and surface diffusion at 230°C (D_B=6.03947×10^{-21} cm^2/s, D_{gb}=7.05988×10^{-13} cm^2/s (assuming δ=0.5nm), and D_s=3.04486×10^{-10} cm^2/s) were inserted into $x \sim \sqrt{Dt}$ and calculated.

If bulk diffusion predominates, the vacancies can travel a distance of 5.50×10^{-13}m. Therefore, assuming the effective volume (the volume from which vacancies can diffuse to the void) to be a quarter sphere of radius r= 5.495×10^{-13}m, gives V=1.738

Table 5. 5: The pre-exponential term for bulk, grain boundary, and surface diffusion [7].

Bulk (D_B)	$0.5\exp\left(-\frac{17T_m}{T}\right)$	cm^2/s
Grain Boundary (δD_{gb})	$1.5\times10^{-8}\exp\left(-\frac{8.9T_m}{T}\right)$	cm^3/s
Surface (D_s)	$0.014\exp-\left(-\frac{6.54T_m}{T}\right)$	cm^2/s

Table 5.6: Activation energies for bulk, grain boundary, and surface diffusion [7]. Units in eV.

ΔH_B	ΔH_{GB}	ΔH_S
2.3	1.2	0.5

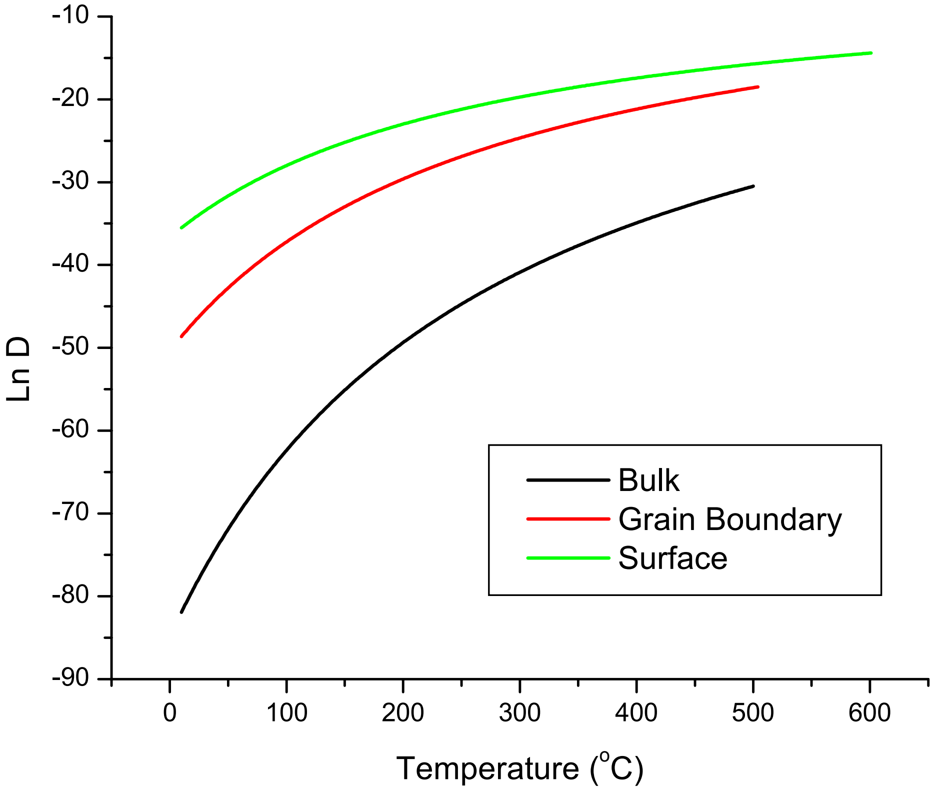


Fig. 5. 9: Plot of ln D versus Temperature for Cu for surface, grain boundary, and bulk (lattice) diffusion.

$10^{-37}m^3$. As in this volume there are 1.473×10^{-8} atoms, assuming the concentration of vacancies, there are not enough vacancies previously calculated, to nucleate a quarter sphere void of 3 nm radius.

If, on the other hand, grain boundary diffusion dominates, the vacancies can travel a distance 5.941 nm in 0.5 seconds. Hence, assuming the effective volume to be a quarter disk, 0.5 nm in width and radius r=5.941nm, gives V=$1.386\times10^{-26}m^3$. As in this volume there are 7.70×10^3 atoms (assuming the grain boundary to have the same structure as the bulk material), there are still not enough vacancies to nucleate a void of 3 nm in size.

However, voids are known to form at the Cu/Ta DB/Cu grain boundary triple junction at the Cu/SiN$_x$ interface, which is known to have a large number of defects due to the CMP process post-electroplating. Thus, this interface needs to be considered. The Cu/SiN interface diffusivity is approximately $\delta_I D_I(m^3/\sec)\approx10^{-27}$ [46]. Using an interface thickness of 0.5 nm, the effective distance traveled by vacancies within a nucleation time of 0.5 seconds is approximately 1 nm. From Fig. 5.2, this gives a volume of V= $1.571\times10^{-27}m^3$. As in this volume there are 8.73×10^2 atoms (assuming the interface to have the same structure as the bulk material), there are still not enough vacancies to nucleate a void 3nm in size.

If we now combine the grain boundary and Cu/SiN$_x$ interface effects, the number of vacancies at the void is approximately 1.085×10^4 by assuming vacancy volume to be $1.422 \times 10^{-30} m^3$. While the number of possible vacancies does exceed the 2400 number of vacancies required for void nucleation, a quantitative understanding of the defects at the Cu/SiN_x is not available at this time.

Finally, if surface diffusion dominates (due to the presence of a free surface in the TEM sample), vacancies can travel a distance of 12.34 microns. This produces an effective volume which can generate enough vacancies to promote the formation of a void 3 nm in size.

In summary what is not clear at this time is the role of defects in the material. It is important to point out that for Cu interconnects, where Cu is electroplated, there is a large number of defects (including contaminants from the electroplating bath) present due to processing. Thus, while the above treatments provide fundamental information regarding the vacancy concentration and effective volume for vacancy diffusion, a more detailed look considering the presence of other defects could be important in understanding the SIV behavior. In addition, the energetics of void formation discussed in 5.2.1 could also be affected by the presence of oxides, excess vacancies, or contaminants, and should be studied further.

5.2.5 Summary for void formation

We have thus far looked at the various possible mechanisms to explain void nucleation at the Cu/Ta DB/Cu grain boundary triple junction. The effects of energetics, grain orientation, diffusion paths, local stresses (stress gradients), and defect (vacancy) concentration were all considered as factors influencing void nucleation.

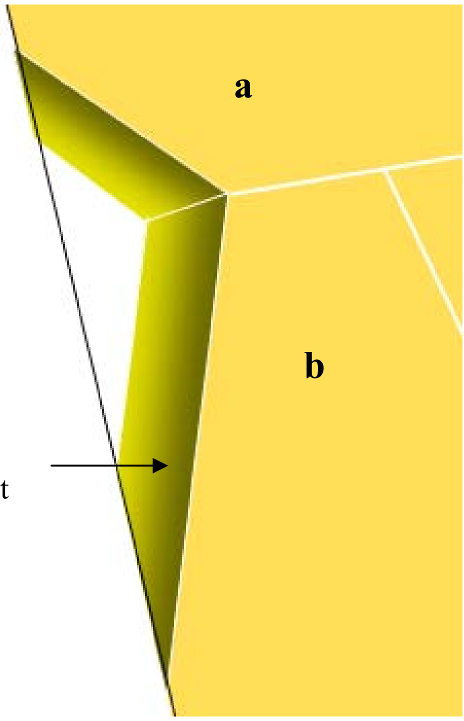
The reason why voids predominantly nucleate at the Cu/Ta DB/Cu grain boundary triple junction could be due to the flux divergence, as the three interfaces (Cu/Ta, Cu grain boundary, Cu/SiN$_x$) exhibit different diffusivities. In addition, the large number of Cu/Ta DB/Cu grain boundary triple junction, the high local stresses at the triple junction, and the density defects (excess vacancies, contaminants, etc.) could all contribute to preferential nucleation of voids at triple junctions. Although there does not seem to be sufficient vacancies in the effective volume for vacancy condensation based on the calculation for the equilibrium number of vacancies under stress, the actual number of vacancies will be much higher than the equilibrium vacancy concentration due to Cu processing (i.e. CMP) Thus a quantitative understanding of vacancy concentration at the Cu/SiN$_x$ interface is crucial to better understand this behavior.

5.3 VOID GROWTH

5.3.1 Crystallographic observations of void surfaces

Upon nucleation, all the voids observed exhibit a spherical surface (Fig. 4.6). This is probably due to the fact that during the very initial stages of void growth, the driving force is very high leading to high vacancy diffusion. As a result, the void tries to minimize surface energy by assuming a spherical shape. However, as the void grows, as for example shown in Fig. 4.9, the driving force is reduced, thereby reducing vacancy diffusion. In this case, a quasi-equilibrium condition is reached, by which the void can expose low energy surfaces. Therefore, the shape of the void changes from spherical to faceted, assuming a particular angle, until the void stops growing. In the case of Al, a similar behavior was found, where the faceted {111} planes were exposed, due to their low surface energy [27]. For Cu, we expect the faceted planes to be the same due to the fact that both Cu and Al possess a face-centered-cubic structure.

A careful look at one of the voids is shown in Fig. 5.7 (a). In this case, when the void opens up and assumes a faceted shape, the void seems to slope downward, as seen in the illustration depicted in Fig. 5.10. Based on these images, the approximate orientation of both open surfaces can be measured. From crystallographic



The exposed surfaces are slanted from right to left at a high angle

Fig. 5. 10: Schematic illustration of the void free surface in Fig. 5.5 (a)

observations, the void develops $(1\bar{3}1)$ and $(02\bar{2})$ surfaces.

For the case of the void in Fig. 5.7(b) a careful analysis revealed that the exposed surfaces are $(0\bar{2}4)$ and $(\bar{1}1\bar{1})$ surfaces. These planes form an angle close to 90^{o} to a direction normal to the two grains. Finally, for the void shown in Fig. 5.7(c), $(1\bar{1}3)$ and $(\bar{1}1\bar{1})$ surfaces opened up during void growth.

Based on the analysis of these three voids, it seems that most of the surfaces that open up during void growth seem to be low surface energy planes (Table 5.7).

5.3.2 Void angle

The void angle commonly observed in this work for faceted voids during void growth was around 140^{o} observed from the direction normal. This value was slightly larger than the angles observed for Al, which were closer to 120^{o} [27]. At equilibrium, the angle exhibited by the void should be given by a relationship between the grain boundary energy and the free surface energy where,

$$E_g = 2E_s \cos(\theta/2) \tag{2.7}$$

Assuming the range of free surface energies and grain boundary energies for Cu (Table 5.1), the void angle vs. surface energy for possible Cu grain boundary energies

Table 5.7: Comparison of low surface energy planes in Cu [96].

(hkl)	E_s (J/m^2)
(111)	1.409
(002)	1.651
(022)	1.641
(113)	1.645
(133)	1.624
(024)	1.713

is plotted in Fig. 5. Based on these calculations, it can be seen that for a void angle of 140 °, and a grain boundary energy of 1.0 J/m^2 (the maximum grain boundary energy) for reported Cu from reference [96]), we get a free surface energy of around 1.4 J/m^2, which is the lower limit according to the free surface energy range assumed (Fig. 5.11).

However, typically voids do not open up free surfaces parallel to the z-direction unless a low surface energy plane is associated with that surface. More likely, voids create slanted free surface (Fig. 5.10). In such a case, the void angle is slightly higher than the 140 ° measured from planar TEM images. Under these conditions, although the free surface energy calculated is still at the lower end of the free surface energy range assumed, it agrees well with the fact that during void growth the free surfaces which are expected to open up are low energy surfaces.

5.3.3 Void growth rate

Void propagation was also monitored by *in-situ* TEM, as shown by the sequence of images taken over a 12 minute period (Fig.4.9). The kinetics of void growth match well with a one-dimensional grain boundary diffusion model, for which the flux, J was calculated using $\mathbf{J} = \frac{\mathbf{D_{gb}}}{\mathbf{kT}} \frac{\partial \sigma_{\mathbf{n}}}{\partial \mathbf{s}}$ [14], where D_{gb} is the grain boundary diffusion coefficient, k is Boltzmann's constant, T the temperature, σ_n the stress normal to the grain boundary, and *s* the distance traveled by the void parallel to the grain boundary

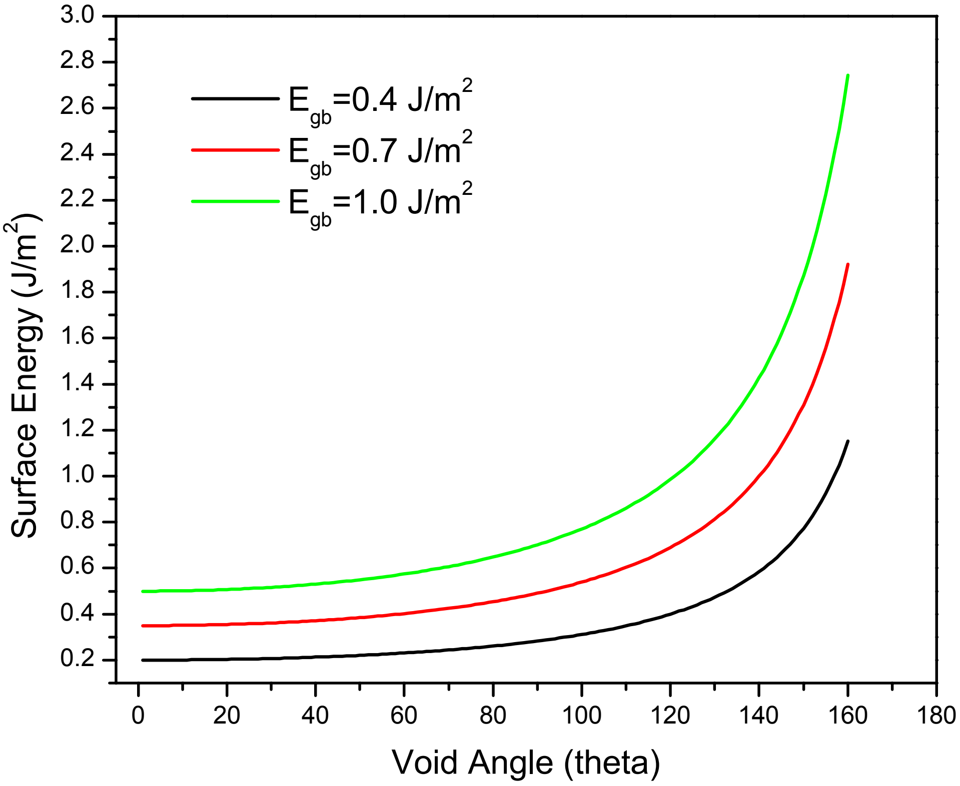


Fig. 5. 11: Plot of void angle vs. surface energy for range of grain boundary energies.

direction. For the calculations, the stress gradient along the grain boundary was considered linear from the intersection of the void and the grain boundary (point P_1 in Fig.4.9), to where the grain boundary intersects the Ta DB (point P_2 in Fig.4.9). For these conditions, the calculated flux was found to be $J=6.6\times10^{19}/m^2s$ and the velocity v=0.66 nm/s. The calculated velocity compares well with the velocity v=0.23 nm/s for void growth observed along the grain boundary direction (Fig.4.9). Based on the calculations, it seems the void growth observed matches closely what would be expected for grain boundary diffusion. This is in agreement with what Gan has reported for stress relaxation in Cu films, which stated that the diffusivity at the Cu/SiN cap layer interface was found to be generally lower than the grain boundary diffusion at the temperature range studied (200°C) [46]. Since the temperature range is very close (compared to 220°C-250°C in this study), the theory might be applicable to void growth in the 180 nm Cu interconnects observed in this study, where faster diffusion rates at the grain boundary could have dominated the void growth rate, above. If diffusion through the Cu grain boundary is an important diffusion mechanism for stress relaxation in Cu, then the models presented in Chapter 2 should be applicable to the case of Cu.

5.3.4 Role of grain boundaries

Some grain boundaries were seen to act as obstacles to void growth, while some grain boundaries were permeable to void growth. Examples of grain boundaries acting as obstacles are observed in Fig. 4.9 and Fig. 4.29. In Fig. 4.9, both types of grain boundaries can be observed. Though the crystal orientation was not measured in this case, the surface energy of the grain boundary will most likely determine whether the void will continue to grow. If the free surface of the newly exposed grain exhibits a fast diffusion path (e.g. (111) plane), then the void will continue to expand. On the other hand if the newly exposed grain exhibits a high energy plane with slow diffusivity, the void is likely to stop. Fig. 4.29 is another good example of how a grain boundary can limit void growth. The presence of such a grain boundary seems to prevent void growth along the width of the line, which leads to a situation where the void opens up with a high void angle.

5.3.5 Summary for void growth

The observations of void growth showed that the flux rate coincides with what would be expected for grain boundary diffusion, despite the presence of a free Cu surface at the bottom of the Cu interconnect due to the TEM sample preparation process. Although, most likely, that some diffusion occurred along the free Cu surface accelerating the void growth process, grain boundary diffusion still seems to be an effective path for diffusion in the void growth process. The main reason for this could be due to the high stress gradient along the width of the line at the tip of the void as was seen in Fig. 4.27. Although such stress gradients also exist along the length of the line at the tip of the void on the Cu/Ta interface (Fig. 4.26), the slow diffusivity of the

Cu/Ta interface does not make this an effective diffusion path. The simulated stresses along the width of the void seems to agree well with the model for void growth presented by Yost [58] in section 2.3.2

In addition, the equilibrium void angle was observed to be slightly larger than 140^o, which seems to match well with the expected high grain boundary energy and low surface energy of Cu. Although the free Cu surface exposed during void growth did not coincide with a {111} type plane, other low energy free surfaces were created during void growth. Void growth also showed that grain boundaries can act as obstacles to grain growth in some cases, preventing the void from propagating to point of failure by growing fully across the width.

Since grain boundary diffusion seems to play an important role in void growth, void growth behavior could be sensitive to the activation energy of grain boundary diffusion as was suggested by Yost's model [57]. A closer study on the effects of the grain boundary type and void growth could provide better insight on this effect.

5.4 THICKNESS CONTRAST FROM STEM

The results from the *in-situ* STEM results showed that post-void formation (Fig. 4.27), a mass pileup resulting in about a 50% increase in thickness from an original thickness of approximately 50 nm could be identified. Since this change in thickness is too large to be accommodated by the Cu/SiN$_x$ interface, this indicates that the material diffused onto the free Cu surface during *in-situ* TEM heating.

In Fig. 4.30 however, a significant sized void had formed (close to 180 nm in width), but no increase in brightness adjacent to the voids were observed, indicating the absence of any accumulation of material on the free surface. In fact, as shown by arrows, a decrease in brightness was observed, showing that the thickness at the edge of the void decreased due to the void propagation. This can be explained by the expected high stresses at these tips, as was shown by FEM stress simulations of a voided Cu interconnect in Fig. 4.25. The high stress concentrations will likely cause a high chemical potential gradient inducing flux of vacancies to the tips resulting in further void growth.

In addition to these two observations, another void was observed in the HAADF STEM mode in-situ during heating conditions, where a small void (approximately 70 by 20 nm) was seen nucleating and undergoing growth at the Cu/Ta interface (Fig. 4.28). As this was seen in the HAADF STEM mode, the grain boundaries present were not clear. It was observed later in BF TEM mode (Fig. 4.29) that the void originated at the triple junction, and propagated laterally in the y-direction, but the presence of the grain boundary prevented further growth of the void along the width. In the observation of the image sequence in Fig. 4.28 taken over a 4 minute period, no noticeable change in the contrast (and thus no noticeable change in thickness) was observed. However, the resolution was poor and no definitive conclusions can be drawn at the moment. However, since the two voids, which did not fully open, did not reveal change in thickness near the void, this could be an indication that grain boundary diffusion might be the initial dominant diffusion path during void growth, as the void tip will have the highest stress concentration (Fig. 4.25). This in turn will make void growth along the width favorable. Once the void fully opens, the stress concentration at the tip of the void no longer exists, and the void might then grow through surface or interface diffusion, resulting in a pileup of material after full void formation.

CHAPTER 6: CONCLUSIONS AND SUGGESTIONS FOR FUTURE WORK

6.1 CONCLUSIONS

This thesis studied the stress relaxation mechanisms in 1.8 micron and 180 nm wide Cu interconnects through the use of *in-situ* TEM heating, and specifically looked at the stress-induced-void formation in 180 nm Cu. The following conclusions were made based on this research.

1. 1.8 micron wide Cu interconnects exhibited distinctly different initial stress relaxation behavior compared to 180 nm Cu interconnects when observed through *in-situ* TEM heating. 1.8 micron wide Cu interconnects exhibited stress relaxation through dislocation nucleation, while the 180 nm Cu interconnects relaxed the stress through void formation. Voids in 180 nm Cu interconnects predominately formed at the Cu/Ta DB/Cu grain boundary triple junctions at temperatures between 220°C and 250°C.

2. Crystal orientation measured with ACT showed that the top layer of the 180 nm Cu interconnects does not have a very strong (111) texture, due to many

contributions from the sidewall texture and annealing twins. The use of the ACT software allowed for the crystal orientation analysis of all grains including nanoscale grains (~20nm).

3. Based on FEM stress calculations and *in-situ* TEM heating results, a correlation between the local stress (gradient) and void formation did exist, although the presence of local stresses does not seem to be the sole reason for void formation. Based on modeling void nucleation, the energetics for void formation alone does not seem to be the responsible mechanism. A more complicated void nucleation process affected by the influence of various defects, grain boundary misorientation, and diffusivity is likely to occur.

4. The nucleation of voids at the Cu/Ta DB/Cu grain boundary triple junction could be due to flux divergence, as the three interfaces (Cu/Ta, Cu grain boundary, Cu/SiN_x) associated with the triple junction exhibit different diffusivities. In addition, the large number of the Cu/Ta DB/Cu grain boundary triple junctions, the high local stresses at the triple junctions, and the density of defects (excess vacancies, contaminants, etc) could all contribute to voids preferentially nucleating at triple junctions.

5. Void growth showed that the flux rate coincides with what would be expected for grain boundary diffusion. During void growth, a constant void angle of 140^{o} was observed to exist. The free faceted surfaces created during void growth does not seem to coincide with a (111) type surface, but does seem to match other low surface energy planes, based on the crystal orientation measurements.

6. The use of the HAADF STEM for identifying thickness changes was demonstrated. In-situ HAADF STEM heating showed that initially, no apparent pile up of material was seen during void growth, but an increase in thickness, adjacent to the void, was observed after complete failure, which indicates that some pile-up of material has occurred.

6.2 FUTURE WORK

One drawback of the experiments conducted in this work is the unavoidable creation of a Cu free surface due to the TEM sample fabrication process. The availability of a fast diffusion path makes it difficult to correlate the empirical observations with theory. In order to improve our understanding, thinner Cu interconnects (<100nm) which will allow the fabrication of TEM samples without having to sacrifice the bottom DB are being considered for collaborative research with Freescale Semiconductors. Experimental results using such samples should provide much better insight into SIV behavior.

This work was concentrated on the effects of the crystal orientation and simulated local stresses on the SIV mechanisms. In addition to SIV, however, Electromigration (EM) is another reliability issue of major concern. In this regard, the experimental methods developed in this thesis could provide valuable information for understanding EM behavior as well. In order to conduct in-situ EM tests in a TEM by applying a small current through the Cu however, the Cu samples must be specifically processed for this test, which makes it difficult to do.

In this respect, a novel method of preparing simple test structures for EM testing in the TEM was developed by the author. In order to apply an electrical current through the TEM samples, additional preparation steps need to be performed for TEM specimens obtained for plan view. In particular, electrodes need to be made on the sample in order to connect the Cu interconnect lines. The steps followed for the fabrication of electrodes are outlined in Fig. 6.1 (steps 1 through 6). To fabricate the electrodes onto the TEM sample, the FIB is used.

First, a carbon tape (1mm by 5mm) is applied on the central part of the TEM samples, so that the long end of the tape is perpendicular to the Cu lines (Step 1). In Step 2, a Pt layer is then sputtered onto the sample by sputtering. The carbon tape in the middle of the section will prevent the Pt from being sputtered on the whole specimen surface. Subsequently, a rectangular box (10microns× 800microns) is milled using the FIB on each side of the C tape, exposing the Cu lines (Step 3). Then, Pt is deposited by FIB to cover the exposed Cu and allow conduction with the initially sputtered Pt layer (Step 4). After removing the sample from the FIB, an additional layer of Pt is sputtered to ensure contact of the Pt layer with the Cu (Step 5). Subsequently, the C tape is removed, allowing the applied current to flow from the electrode to electrode through the Cu lines (Step 6). The absence of the Pt layer in the middle of the sample prevents any current from flowing on the surface (Fig. 6.1)

Fig. 6.2 shows an SEM image of a TEM sample prepared by the author after the aforementioned steps have been completed, while Fig.10.b shows a magnified image of the electrode's contact with the Cu interconnects. The conducting C tape has been left on to prevent electron noise in the SEM. Testing of the completed sample in air showed stable current flow through the Cu interconnect lines.

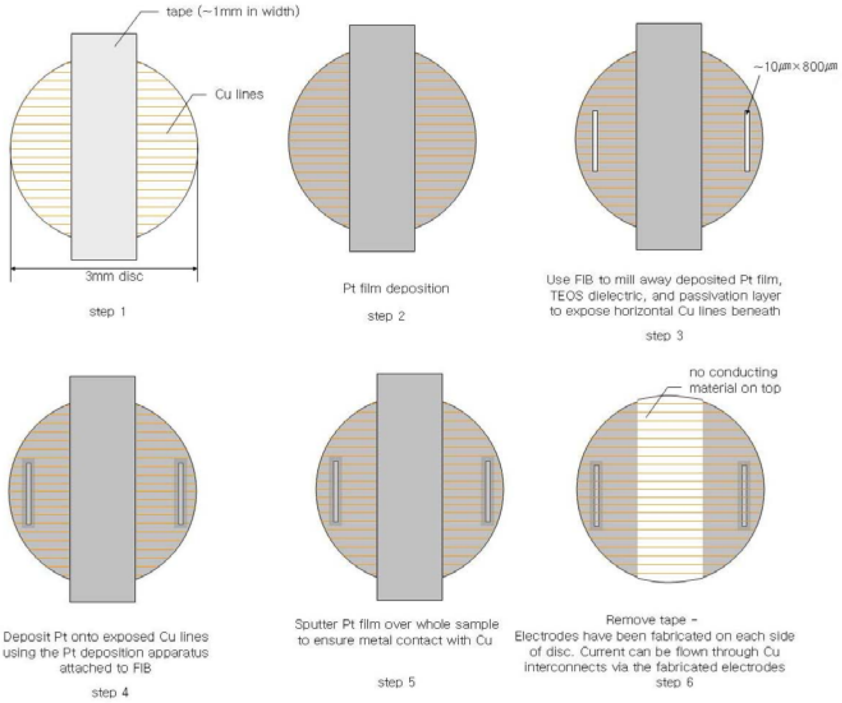
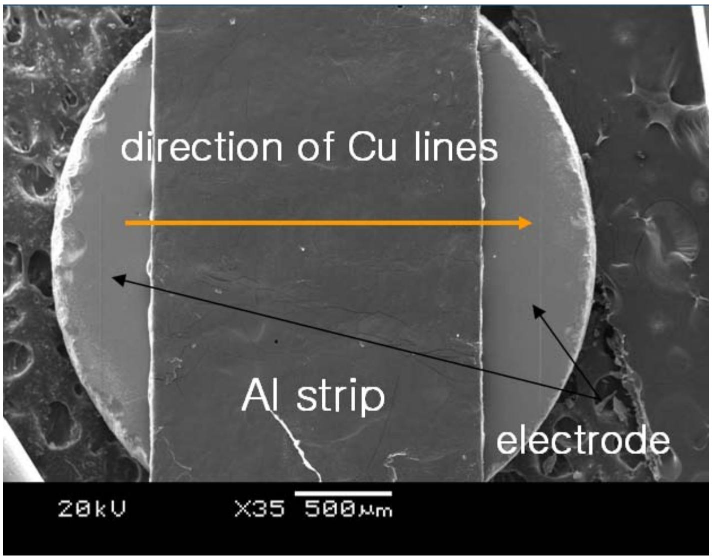
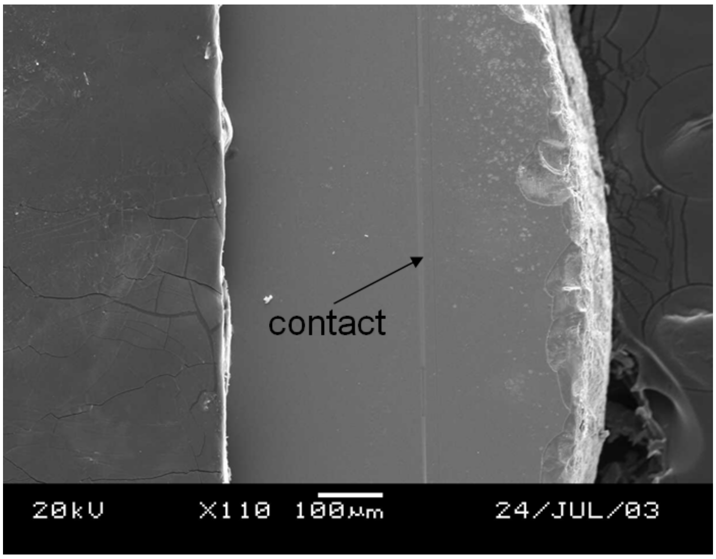


Fig. 6.1: Schematic diagram showing the 6 steps for fabricating electrodes on Cu interconnects for *in-situ* TEM applied electrical field experiments.



(a)



(b)

Fig. 6.2: (a) SEM image of TEM sample used for *in-situ* TEM applied electrical field experiments. (b) Magnified image of electrode. Contact between Cu and electrode can be seen.

REFERENCES

[1] G. Moore, “Cramming more components onto integrated circuits”, *Electronics* **38** (1965)

[2] http://www.intel.com/technology/mooreslaw/index.htm

[3] P. Pai, C. Ting, “Copper as the Future Interconnection Material”, *Proc. of the VMIC* (1989) 258-264

[4] D. Edelstein, J. Heidenreich, R. Goldblatt, W. Cote, C. Uzoh, N. Lustig, P. Roper, T. McDevittt, W. Motsifft, A. Simon, J. Dukovic, R. Wachnik, H. Rathore, R. Schulz , L. Su, **S.** Lucet, J**.** Slatteryt, “Full Copper Wiring in a Sub-0.25 ㎛ CMOS ULSI Technology”, *IEEE Proceedings of the IEDM* (1997) 773-776

[5] The National Technology Roadmap for Semiconductors, *Semiconductor Industry Association* (2005)

[6] http://www-03.ibm.com/press/us/en/attachment/21479.wss?fileId= ATTACH_FILE2&filename=airgapsem1r.jpg

[7] D. Ohring, *Materials Science of Thin Films : Deposition & Structure*, Academic Press (2002)

[8] M. Ohring, *Reliability and Failure of Electronic Materials and Devices*, Academic Press (1998)

[9] S.P. Riege, J.A. Prybyla, A.W. Hunt, "Influence of Microstructure on Electromigration Dynamics in Submicron Al Interconnects: Real-Time Imaging", *Applied Physics Letters* **69** (1996) 2367-2369

[10] Z. Zhang, Z. Suo, J. He, "Saturated Voids in Interconnect Lines due to Thermal Strains and Electromigration", *Journal of Applied Physics* **98** (2005) 074501

[11] C. Hu, K. Rodbell, T. Sullivan, K. Lee, D. Bouldin, "Electromigration and Stress-Induced Voiding in Fine Al and Al-alloy Thin-film Lines", *IBM J. Res. Dev.* **39** (1995) 465-497

[12] J. Lloyd, J. Clement, "Electromigration in Copper Conductors", *Thin Solid Films* **262** (1995)135-141

[13] J. Proost, T. Hirato, T. Furuhara, K. Maex, J. Celis, "Microtexture and Electromigration-Induced Drift in Electroplated Damascene Cu", *Journal of Applied Physics*, **87** (2000) 2792-2802

[14] K.D. Lee, E. Ogawa, H. Matsuhashi, P. Justison, K.S. Ko, P. H, V. Blaschke, "Electromigration Critical Length Effect in Cu/Oxide Dual-Damascene Interconnects", *Applied Physics Letters*, **79** N20 (2001) 3236-3238

[15] O. Kraft, E. Arzt, "Current Density and Line Width Effects in Electromigration: A New Damage-Based Lifetime Model", *Act Materialia* **46** (1998) 3733-3743

[16] J. Loyd, M. Lande, E. Liniger, "Relatioship between Interaction Adhesion and Electromigration in Cu Metallization", *IEEE IRW Final Report* (2002) 32-35

[17] S. Fujisawa, T. Kikkawa, T. Kizuka, “Direct Observation of Electromigration and Induced Stress in Cu Nanowire”, *Japanese Journal of Applied Physics* **42** (2003) L1433-L1435

[18] J. Sanchez Jr., L. McKnelly, J. Morris Jr., “Morphology of Electromigration-Induced Damage and Failure in Al Alloy Thin Film Conductors ”, *Journal of Electronic Materials* **19** (1990) 1213-1220

[19] J.W. McPherson, C.F. Dunn, “A Model for Stress-Induced Metal Notching and Voiding in Very Large-Scale-Integrated Al-Si(1%) Metallization”, *Journal of Vacuum Science and. Technology* **B5** (1987) 1321-1325

[20] A. Sekiguchi, J. Koike, S Kamiya, M. Saka, and K. Maruyama, “Void Formation by Thermal Stress Concentration at Twin Interfaces in Cu Thin Films”, *Applied Physics Letter* **79** (2001) 1264-1266

[21] R. Gleixner, B. Clemens, W. Nix, “Void Nucleation in Passivated Interconnect Lines : Effects of Site Geometries, Interfaces, and Interface Flaws”, *Journal of Materials Research* **12** (1997) 2081-2090

[22] A. Wikstreom, P. Gudmundson, S. Suresh, “Analysis of Average Thermal Stresses in Passivated Metal Interconnects”, *Journal of Applied Physics* **86** (1999) 6088-6095

[23] J. Koike, M. Wada, M. Sanada, K. Maruyama, “Effects of Crystallographic Texture on Stress-Migration Resistance in Copper Thin Films”, *Applied Physics Letters* **81** (2002) 1017-1019

[24] H. Park, S. Hwang, Y. Joo, “Stress-Induced Surface Damage and Grain Boundary Characteristics of Sputtered and Electroplated Copper Thin Films”, *Acta Materialia* **52** (2004) 2435-2440

[25] E. Ogawa, J. McPherson, J. Rosal, K. Dickerson, T. Chiu, L. Tsung, M. Jain, T. Bonifield, J. Ondrusek, W. McKee, “Stress-Induced Voiding under Vias Connected to Wide Cu Metal Leads”, *Proc. of the IRPS 2002* 312-321

[26] C. Hu, K. Rodbell, T. Sullivan, K. Lee, D. Bouldin, “Electromigration and Stress-Induced Voiding in Fine Al and Al-alloy Thin-film Lines”, *IBM J. Res. Dev.* **39** (1995) 465-497

[27] H. Okabayashi, “Stress-Induced Void Formation in Metallization for Integrated Circuits”, *Materials Science and Engineering* **R11** (1993) 191-241

[28] P. Borgesen, J. Lee, R. Gleixner, C. Li, “Thermal Stress-Induced Voiding in Narrow, Passivated Cu Lines”, *Applied Physics Letter* **60** (1992) 1706-1708

[29] R. Keller, S. Baker, E. Arzt, “Stress Temperature Behavior of Unpassivated Thin Copper Films”, *Acta Materialia* **47** (1999) 415-426

[30] D. Gan, S. Yoon, P. Ho, “Effects of Passivation Layer on Stress Relaxation in Cu Line Structures”, *Proc. of the IITC 2002* 180-182

[31] D. Josell, T. Weish, H. Gao, “Diffusional Creep: Stresses and Strain Rates in Thin Films and Multilayers”, *MRS Bulletin* **January** (2002) 39-44

[32] G. Dehm, D. Weiss, E. Arzt, "In situ TEM Study of Thermal-Stress-Induced Dislocation in a Thin Cu Film Constrained by a Si Substrate", *Materials Science and Engineering* **A309-310** (2001) 468-472

[33] R. Vinci, E. Zielinski, J. Bravman, "Thermal Strain and Stress in Copper Thin Films", *Thin Solid Films* **262** (1995) 142-153

[34] M. Thouless, J. Gupta, J. Harper, "Stress Development and Relaxation in Copper Films During Thermal Cycling", *Journal of Materials Research* **8** (1993) 1845-1852

[35] P. Flinn, "Measurement and Interpretation of Stress in Copper Films as a Function of Thermal History", *Journal of Materials Research* **6** (1991) 1498-1501

[36] Kraft, L. Freund, R. Phillips, E. Arzt, "Dislocation Plasticity in Thin Metal Films", *MRS Bulletin* **January** (2002) 30-37

[37] D. Gan, G. Wang, P. Ho, "Effects of Dielectric Material and Linewidth on Thermal Stresses of Cu Line Structures", *Proc. of the IITC 2002* 271-273

[38] E. Ege, Y. Shen, "Thermomechanical Response and Stress Analysis of Copper Interconnects", *Journal of Electronic Materials* **32** (2003) 1000-1011

[39] I. Dutta, M. Chen, K. Peterson, T. Shultz, "Plastic Deformation and Interfacial Sliding in Al and Cu Thin Film: Si Substrate Sysmtems due to Thermal Cycling", *Journal of Electronic Materials* **30** (2001) 1537-1548

[40] M. Doerner, W. Dix, “Stresses and Deformation Processes in Thin Films on Substrates”, *CRC Critical Reviews in Solid State and Materials Sciences* **14** (1988) 225-268

[41] M. Korhonen, R. Black, C. Li, “Stress Relaxation of Passivated Aluminum Line Metallizations on Silicon Substrates”, *Journal of Applied Physics* **69** (1991) 1748-1755

[42] B. Clemens, J. Bain, “Stress Determination in Textured Thin Films Using X-Ray Diffraction”, *MRS Bulletin* **July** (1992) 46-51

[43] R. Vinci, E. Zielinski, J. Bravman, “Thermal Strain and Stress in Copper Thin Films”, *Thin Solid Films* **262** (1995) 142-153

[44] R. Keller, S. Baker, E. Arzt, “Quantitative Analysis of Strengthening Mechanisms in Thin Cu Films: Effects of Film Thickness, Grain Size, and Passivation”, *Journal of Materials Research* **13**(1998) 1307-1317

[45] M.A. Korhonen, P. Borgesen, Che-Yu Li, “Mechanisms of Stress-induced and Electromigration-induced Damage in Passivated Narrow Metallizations on Rigid Substrates”, *MRS Bulletin* **July** (1992) 61-68

[46] D. Gan, P. Ho, R. Huang, J. Leu, J. Maiz, . Scherban, “Isothermal Stress Relaxation in Electroplated Cu Films. I. Mass Transport Measurements”, *Journal of Applied Physics* **97** (2005) 103531

[47] S. Rhee, “Thermal Stress Behaviors of Al(Cu)/low-k and Cu/low-k Submicron Interconnect Structures”, *PhD Dissertation, UT Austin* (2001)

[48] B.J. Inkson, G. Dehm, T. Wagner, “In situ TEM Observations of Dislocation Motion in Thermally Strained Al Nanowires”, *Acta Materialia* **50** (2002) 5033-5047

[49] T.J. Balk, G. Dehm, E. Arzt, “Parallel Glide : Unexpected Dislocation Motion Parallel to the Substrate in Ultrathin Copper Films”, *Acta Materialia* **51** (2003) 4471-4485

[50] G. Dehm, E. Arzt, “In Situ TEM Study of Dislocations in a Polycrystalline Cu Thin Film Constrained by a Substrate”, *Applied Physics Letters* **77** (2000) 1126-1128

[51] G. Dehm, D. Weiss, E. Arzt, “*In-situ* TEM Study of Thermal-Stress-Induced Dislocations in a Thin Cu Film Constrained by a Si Substrate”, *Mat. Sci. and Eng.* **A309-310** (2001) 468-472

[52] V. Weihnacht, W. Bruckner, “Dislocation Accumulation and Strengthening in Cu Thin Films”, *Acta Materialia* **49** (2001) 2365-2372

[53] B. von Blanckenhagen, E. Arzt, P. Gumbsh, “Discrete Dislocation Simulation of Plastic Deformation in Metal Thin Films”, *Acta Materialia* **52** (2004) 773-784

[54] J. Curry, G. Fitzgibbon, Y. Guan, R. Muollo, G. Nelson, A. Thomas, “New Failure Mechanisms in Sputtered Aluminum Silicon Films”, *Proc of the IEEE Reliability Physics Symposium 1984* 6-8

[55] J. Yue, W. Funsten, R. Taylor, “Stress Induced Voids in Aluminum Interconnects During IC Processing”, *Proc. of the IEEE Reliability Physics Symposium 1985* 126-137

[56] H. Kaneko, M. Hasunuma, A. Sawabe, T. Kawanoue, Y. Kohanawa, S. Komatsu, M. Miyauchi, “A Newly Developed Model for Stress Induced Slit-Like Voiding”, *Proc. of the IRPS 1990* 194-199

[57] F. Yost, D. Amos, A. Romig Jr., “Stress-Driven Diffusive Voiding of Aluminum Conductor Lines”, *Proc. of the IEEE Reliability Physics Symposium* (1989) 193-201

[58] F. Yost, F. Campbell, “Stress-Voiding of Narrow Conductor Lines”, *Proc. of the IEEE Circuits and Devices* (1990) 40-44

[59] Akio Takaoka, Katsumi Ura, “Stereoscopic Observation and Determination of Surface Orientation of Voids in Stress-Thermal Migrated Aluminum Lines of LSI with UHVEM”, *Ultramicroscopy* **39** (1991) 299-305

[60] M. Kato, H. Niwa, H. Yagi, H. Tsuchikawa, “Diffusional Relaxation and Void Growth in an Aluminum Interconnect of Very Large Scale Integration”, *Journal of Applied Physics* **68** (1990) 334-338

[61] S. Hu, “Stress-driven Void Growth in Narrow Interconnection Lines”, *Applied Physics Letter* **59** (1991) 2685-2687

[62] A. Tezaki, T. Mineta, H. Egawa, “Measurement of Three Dimensional Stress and Modeling of Stress Induced Migration Failure in Aluminum Interconnects”,

P*roc. of the IRPS 1990* 221-229

[63] K. Doong, R. Wang, S. Lin, L. Hung, S. Lee, C. Chiu, D. Su, K. Wu, W Young, Y. Peng, "Stress-Induced Voiding and its Geometry Dependency Characterization", *Proc. of the IRPS 2003* 156-160

[64] J. Nucci, Y. Shacham-Diamand, J. Sanchez Jr., "Effects of Linewidth, Microstructure, and Grain Growth on Voiding in Passivated Copper Lines", *Applied Physics Letter* **66** (1995) 3585-3587

[65] R. Keller, J. Nucci, D. Field, "Local Textures and Grain Boundaries in Voided Copper Interconnects", *Journal of Electronic Materials* **26** (1997) 996-1001

[66] J. Nucci, R. Keller, J. Sanchez Jr., Y. Shacham-Diamand, "Local Crystallographic Texture and Voiding in Passivated Copper Interconnects", *Applied Physics Letter* **69** (1996) 4017-4019

[67] J. Nucci, R. Keller, D. Field, Y. Shacham-Diamand, "Grain Boundary Misorientation Angles and Stress-Induced Voiding in Oxide Passivated Copper Interconnects", *Applied Physics Letter* **70** (1997) 1242-1244

[68] N. Singh, A. Bower, D. Gan, S. Yoon, P. Ho, J. Leu, S. Shankar, "Numerical Simulations and Experimental Measurements of Stress Relaxation by Interface Diffusion in a Patterned Copper Interconnect Structure", *Journal of Applied Physics* **97** (2004) 013539

[69] R. Huang, D. Gan, P. Ho, "Isothermal Stress Relaxation in Electroplated Cu Films. II. Kinetic Modeling", *Journal of Applied Physics* **97** (2005) 103532

[70] Yost, “Voiding due to Thermal Stress in Narrow Conductor Lines”, *Scripta Metallalurgica* **23** (1989) 1323-1328

[71] W-M. Kuschke, A. Kretschmann, R-M. Keller, R.P. Vinci, C. Kaufmann, E. Arzt, “Textures of Thin Copper Films”, *Journal of Materials Research* **13** (1998) 2962-2968

[72] C. Lingk, M. Gross, W. Brown, “X-ray Diffraction Pole Figure Evidence for (111) Sidewall Texture of Electroplated Cu in Submicron Damascene Trenches”, *Applied Physics Letters* **74** (1999) 682-684

[73] J. Cho, H. Lee, H. Kim, J. Szpunar, “Textural and Microstructural Transformation of Cu Damascene Interconnects After Annealing”, *Journal of Electronic Materials* **34** (2005) 506-514

[74] L. Vanasupa, D. Pinck, Y. Joo, T. Nogami, S. Pramanick, S. Lopatin, K. Yang, “The Impact of Linewidth and Line Density on the Texture of Electroplated Cu in Damascene-Fabricated Lines”, *Electrochemical and Solid-State Letters* **2** (1999) 275-277

[75] D. Lee, H. Lee, “Effect of Stresses on the Evolution of Annealing Textures in Cu and Al Interconnects”, *Journal of Electronic Materials* **32** (2003) 1012-1022

[76] H. Lee, H. Han, D. Lee, “Annealing Textures of Copper Damascene Interconnects for Ultra-Large-Scale Integration”, *Journal of Electronic Materials* **34** (2005) 1493-1499

[77] C. Steinbruchel, B. Chin, "Copper Interconnect Technology", *Tutorial Texts in Optical Engineering* **TT46** (2001)

[78] R. Langford, A. Petford-Long, "Preparation of Transmission Electron Microscopy Cross-section Specimens using Focused Ion Beam Milling", *Journal of Vacuum Science and Technology* **A19** (2001) 2186-2193

[79] J. Lee, D. Su, J. Chuang, "A Novel Application of the FIB Lift-out Technique for 3-D TEM Analysis", *Microelectronics Reliability* **41** (2001) 1551-1556

[80] D. Williams, C. Carter, *Transmission Electron Microscopy*, Plenum Press (1996)

[81] ABAQUS User's Manual, version 6.6, 2006. Providence, RI.

[82] T. Courtney, *Mechanical Behavior of Materials*, Mcgraw-Hill (2000)

[83] Haixia Mei, J.H. An, Rui Huang, P.J. Ferreira, "Finite Element Modeling of Stress Variation in Multilayer Thin-Film Specimens for *In-situ* TEM Experiments", *Journal of Materials Research* **22** (2007) 2737-2741

[84] I. Pozsgai, "Mass Thickness Determination and Microanalysis of Thin Films in the TEM-Revisited", *Ultramicroscopy* **107** (2007) 191-195

[85] Klenov, Stemmer, "Contribution to the contrast in Experimental High Angle Annular Dark Field Image", Ultramicroscopy **106** (2006) 889-901

[86] R.J. Keyse, A.J. Garratt-Reed, P.J. Goodhew, G.W. Lorimer, "Introduction to Scanning Transmission Electron Microscopy", Bios Scientific Publishers (1998)

[87] P. Flinn, "Measurement and Interpretation of Stress in Copper Films as a Function of Thermal History", *Journal of Materials Research* **6** (1991) 1498-1501

[88] R. Vinci, E. Zielinski, J. Bravman, "Effect of Copper Film Thickness on Stress and Strain in Grains of Different Orientation", *Mat. Res. Soc. Symp. Proc.* **356** (1995) 459-464

[89] Th. Hehenkamp, W. Berger, J. Kluin, Ch. Ludecke, J. Wolff, "Equilibrium Vacancy Concentration in Copper Investigated with the Absolute Technique", *Physical Review B* **45** (1992)1998-2003

[90] M. Aoyagi, "Modeling of Vacancy Flux due to Stress-Induced Migration", *Journal of Vacuum Science and Technology* B **21** (2003) 1314-1317

[91] R. Bauer, W. Maysenholder, A. Seeger, "Calculations of Point-Defect Properties in Copper, Silver, and Gold Based on Three-Body Interactions", *Physics Letters* **90A** (1982) 55-58

[92] A. Suzuki, Y, Mishin, "Atomistic Modeling of Point Defects and Diffusion in Copper Grain Boundaries", *Interface Science* **11** (2003) 131-148

[93] Mengzhi Pang, Monika Backhaus-Ricoult, and Shefford P. Baker "The Effect of Oxygen on Adhesion of Thin Copper Films to Silicon Nitride" U3.6.1 *Mat. Res. Soc. Symp. Proc.* Vol. 795 (2003)

[94] P. Heino, E. Ristolainen, “Interfaces in Copper Nanoconnections*”, Journal of Vacuum Science and Technology* B **20** (2002) 2052-2057

[95] H.L. Skriver, N.M. Resengaard, “Surface Energy and Work Function of Elemental Metals”, *Physical Review* B **46** (1992) 7157-7168

[96] J.M. Zhang, F. Ma, K. Xu, “Calculation of the Surface Energy of FCC Metals with Modified Embedded-Atom Method”, *Applied Surface Sciences* **229** (2004) 34-42

[97] A. Kiejna, “Surface atomic structure and energetics of tantalum”, *Surface Science* **598** (2005) 276-284

[98] G. Kaptay, E. Bader, L. Bolyan, “Interfacial Forces and Energies Relevant to Production of Metal Matrix Composites”, *Materials Science Forum* **329-330** (2000) 151-156

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